CHAPTER

Conventional H-bridge and recent multilevel inverter topologies

3

Ilhami Colak[a], Ersan Kabalcı[b], and Gokhan Keven[c]

[a]*Department of Electrical and Electronics Engineering, Faculty of Engineering and Architecture, Nisantasi University, Istanbul, Turkey* [b]*Department of Electrical and Electronics Engineering, Faculty of Engineering and Architecture, Nevsehir Haci Bektas Veli University, Nevsehir, Turkey* [c]*Department of Electronics and Automation, Vocational High School, Nevsehir Haci Bektas Veli University, Hacibektas, Nevsehir, Turkey*

3.1 Introduction

Today, generation of electricity from renewable energy sources (RESs) is a key issue in distributed energy generation systems. Photovoltaic (PV) panels, wind turbines, fuel cells, biomass, and other natural sources are used for energy production [1]. RESs help to protect the planet from pollution caused by conventional energy generation systems. In addition, RESs have another advantage in that the energy is produced close to where it is consumed. PVs became commercially viable at the beginning of this century, converting freely available sunlight into electricity cost-effectively [2]. The International Energy Agency (IEA) has reported that the total PV power plant capacity increased by more than 100 GW in 2019 [1, 2]. PV systems are classified into two categories: stand-alone and grid-tied PV systems. The stand-alone PV systems use the energy directly at load sites, but grid-tied systems are connected to the grid for transmission, distribution, and consumption. The percentage of energy produced by grid-tied systems is increasing daily [3].

The inverter converts the energy produced by PV panels from DC to AC. The connection between PV modules and the grid is made in two different ways, with galvanic isolation (with transformer or isolated) and without galvanic isolation (transformerless or nonisolated), as depicted in Fig. 3.1 [3, 4]. Galvanic isolation is provided by using a transformer in the inverter connected to the grid. This type of isolation protects the system and users from hazardous voltages and leakage currents. In addition to this, it reduces the interference of the leakage current and DC injection into the grid. Grid-tied PV systems with a transformer are implemented with a low-frequency (line frequency) or high-frequency transformer-based inverter, shown in Fig. 3.1A and B, respectively. The low-frequency transformers, which are heavy, bulky, and expensive solutions, are located at the AC side of

Multilevel Inverters. https://doi.org/10.1016/B978-0-12-821668-2.00010-6

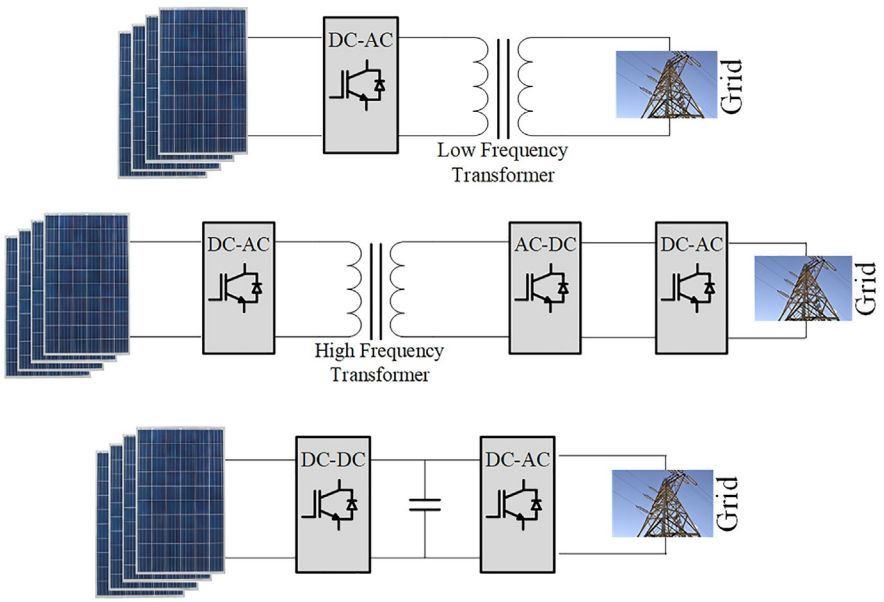

FIG. 3.1

Classification of grid-tied inverters regarding galvanic isolation: (A) low-frequency transformer-based inverter; (B) high-frequency transformer-based inverter; (C) transformerless inverter.

the inverter, while the high-frequency transformer is used on the DC side of the inverter. It should be noted that low-frequency transformers reduce the system efficiency due to power loss in the windings. A crucial reduction in size and weight is obtained with a high-frequency transformer. However, the efficiency of the inverter is still low due to the conversion of energy between DC and AC more than once. Hence, nonisolated inverters are used in PV grid-tied systems owing to their high efficiency, lower cost, and high power density [2–6]. The nonisolated inverter systems do not have any galvanic isolation. Therefore leakage current is higher when compared with the isolated inverters. The leakage current increases the electromagnetic interference (EMI), total harmonic distortion (THD), and the system losses, in addition to safety problems caused by the leakage current [4].

PV inverters are commonly implemented in the H-bridge topology in both isolated and nonisolated systems. The H-bridge topology has four switching components in its traditional structure, which is called H4 topology, and it is not suitable for leakage current for nonisolated inverters. To achieve minimum leakage current, recent improved inverter topologies have emerged, such as H5, the highly efficient and reliable inverter concept (HERIC), and H6 configurations, with additional switching components in their structures [1]. Besides the structure of the inverter, modulation strategies are a very important issue in decreasing the leakage current and improving the output

parameters of an inverter. Sinusoidal pulse width modulation (SPWM) is a common modulation strategy widely used in control of inverters [5].

3.2 H-bridge inverter topology

H-bridge (or full-bridge) inverter topology was patented by Baker et al. [7]. This topology can be used as inverter cells in cascaded multilevel inverters. Other traditional inverter topologies, namely neutral-point clamped and flying capacitor clamped, were invented after the H-bridge topology. As mentioned earlier, the H-bridge topology is typically used as an H4 topology, especially in grid-tied inverter systems where four switches are formed with two legs and each leg has two switches serially connected, as seen in Fig. 3.2A. S_1-S_2 complementary switches

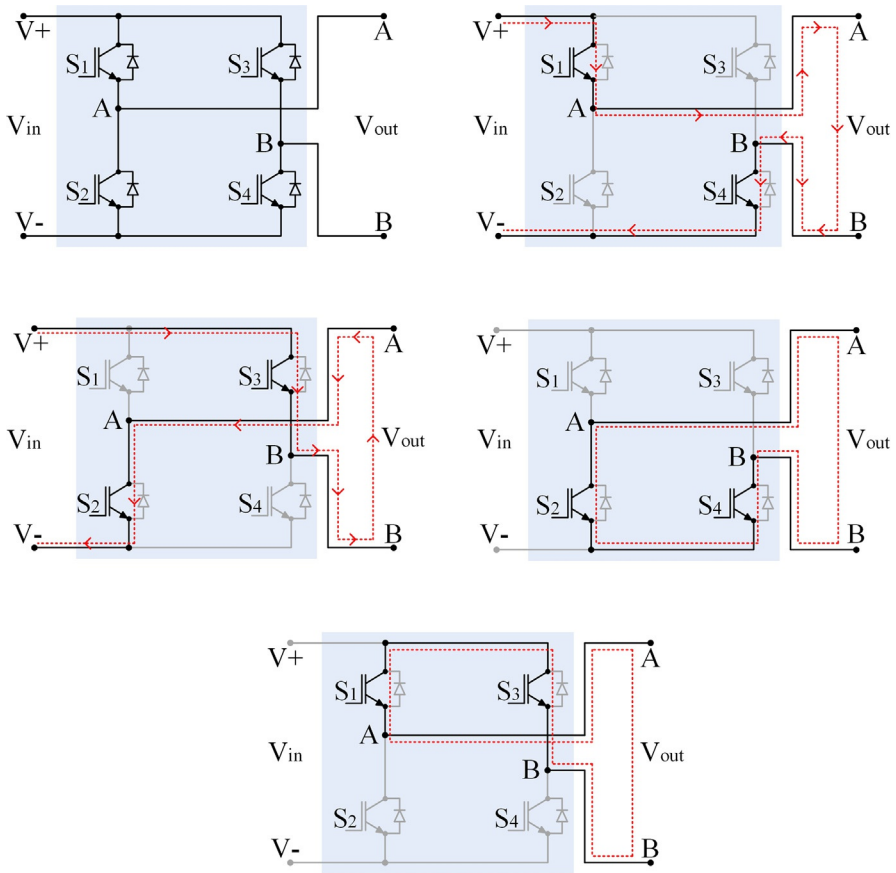

FIG. 3.2

H4 inverter: (A) general structure; (B) positive half-cycle; (C) negative half-cycle; (D) freewheeling mode-I; (E) freewheeling mode-II.

are connected on the same leg, while S_3-S_4 complementary switches are on the other leg. The positive and negative input terminals are connected to batteries or power supplies, and AC output terminals are connected to the middle point of the legs [8, 9].

This inverter generates three different output values, $+V_{DC}$, 0, $-V_{DC}$, for V_{DC} as the input value. The switching orders of the inverter are represented in Fig. 3.2B and C as the "ON" state of S_1 and S_4 switches in the positive half-cycle, and the "ON" state of S_2 and S_3 switches in the negative half-cycle of the AC wave. The zero-voltage state can be achieved in two different freewheeling methods. The S_2 and S_4 switches are turned to the "ON" state in the freewheeling mode-I, as shown in Fig. 3.2D, while the second one is obtained by turning S_1 and S_3 switches "ON" in freewheeling mode-II, as shown in Fig. 3.2E. The output value is "0" in these freewheeling modes [8, 9].

3.3 Common mode voltage and leakage current

H4 and recent H multilevel inverter topologies have been investigated related to analysis parameters in nonisolated multilevel PV inverter systems. The performances of the topologies are compared using parameters such as common mode voltage (CMV), leakage current, efficiency, and THD ratios. The efficiency denotes the conversion ratio between input and output power of the inverter, and the THD parameter is researched with regard to increasing the waveform quality of the inverter and grid [4, 10].

The CMV can be described as the average value of the voltages between the input or output terminals and a common reference. The negative terminal of the inverter (or PV panel) is the reference point (N) of the inverter output. Therefore the CMV of output terminals A and B can be calculated as shown in Eq. (3.1), where V_{AN} and V_{BN} are the voltage values between output terminals (A and B) of the inverter, and N is the reference point of the PV panel. The general diagram for a grid-tied nonisolated inverter with parasitic capacitance for the H4 inverter topology is shown in Fig. 3.3. The Z_G is the ground resistance of grid and parasitic capacitance connected

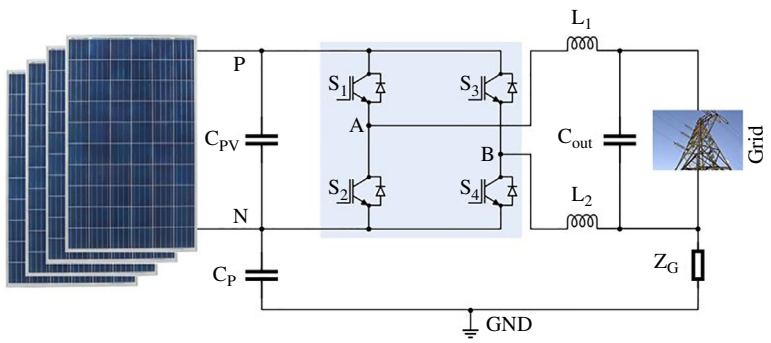

FIG. 3.3

General diagram for a grid-tied nonisolated inverter with parasitic capacitance.

via this resistor to grid. L_1-L_2 and C_{out} are filter components. L_1 and L_2 must have the same value to achieve minimum alternation in CMV [2, 6, 10].

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{3.1}$$

The leakage current is caused by CMV and it is detected from parasitic capacitance (C_P). The C_P occurs between PV modules and the grid as an unwanted side effect. An electrically chargeable surface area is accrued in the PV module that looks like a grounded frame. Therefore a connection occurs between the ground of the grid and PV module via the AC and DC filter elements and the grid impedance in a non-isolated inverter. The effect of C_P depends on many factors, such as the structure of the solar panel and the structure of the frame, surface of the cell, the distance between cells in the PV module, weather conditions, humidity, dust or salt covering the PV panels, etc. Therefore the C_P changes for each PV module under different conditions [4, 6, 10].

A simplified common mode leakage current model can be obtained by replacing the PV panel and switches with two PWM voltage sources (V_{AN} and V_{BN}), as shown in Fig. 3.4. The total leakage current (I_L) can be calculated by using the superposition theorem, which sums the currents in Eq. (3.2). Here, I_{L1}, I_{L2}, and I_{LG} are the leakage currents generated by V_{AN}, V_{BN}, and grid voltage as expressed in Eqs. (3.3)–(3.5), respectively. In these equations, L_1 and L_2 inductors are at the same value and they are used as L. The parameter I_{LG} can be neglected at grid frequency, because the

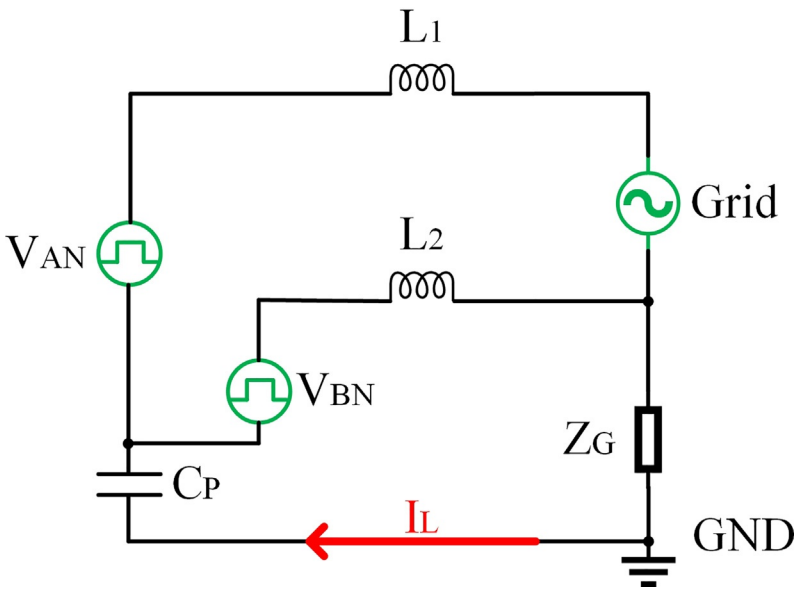

FIG. 3.4

Simplified common mode leakage current model.

leakage current depends on frequency. Therefore Eq. (3.2) can be written as Eq. (3.6). The total leakage current can be calculated in terms of CMV using Eq. (3.7). The equivalent circuits of leakage current (generated by V_{AN}, V_{BN}, and grid) are shown in Fig. 3.5A–C, respectively [2, 10].

$$I_L = I_{L1} + I_{L2} + I_{LG} \tag{3.2}$$

$$I_{L1} = \frac{jV_{AN}}{\frac{2}{\omega C_P} - \omega L} \tag{3.3}$$

$$I_{L1} = \frac{jV_{BN}}{\frac{2}{\omega C_P} - \omega L} \tag{3.4}$$

$$I_{LG} = \frac{-jV_G}{\frac{2}{\omega_g C_P} - \omega_g L} \tag{3.5}$$

$$I_L = \frac{jV_{AN}}{\frac{2}{\omega C_P} - \omega L} + \frac{jV_{BN}}{\frac{2}{\omega C_P} - \omega L} \tag{3.6}$$

$$I_L = \frac{j2V_{CMV}}{\frac{2}{\omega_{CMV} C_P} - \omega_{CMV} L} \tag{3.7}$$

As discussed earlier, the leakage current is generated due to the alternation of the CMV of the inverter. The minimum value of the variation of CMV causes minimum leakage current. Alternation of CMV decreases with the use of bipolar SPWM as a modulation strategy. In this situation, THD increases and the efficiency of the inverter decreases. When the inverter is switched using unipolar SPWM as the

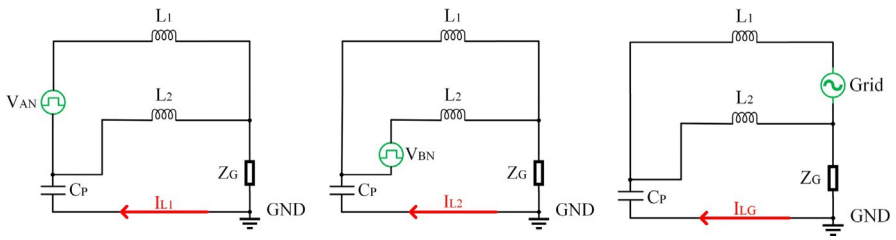

FIG. 3.5

The equivalent circuits of leakage current: (A) generated by V_{AN}, (B) generated by V_{BN}, (C) generated by grid.

Table 3.1 Leakage current values and their corresponding disconnection times.

Leakage current value (mA)	Disconnection time (s)
30	0.3
60	0.15
100	0.04

modulation strategy, alternation of CMV and THD ratios decreases, and the efficiency of the inverter increases. The H4 inverter topology is suitable to be used with two different SPWM modulation strategies, which are introduced in the following section of this chapter [11, 12]. The nonisolated grid-tied inverter systems must conform to some specific standards, such as IEEE 1547.1-2018, VDE0126-1-1, EN 50106, and IEC61727. The VDE0126-1-1 standard limits the RMS value of leakage current to 300 mA. Based on this standard, leakage current values and their corresponding disconnection times are listed in Table 3.1 [2, 13, 14].

3.4 Modulation strategy

Modulation strategy is one of the major factors of the nonisolated grid-tied H-bridge inverter. SPWM is the most commonly used modulation technique for H4 and other H-bridge based multilevel topologies. SPWM is a fundamental modulation method for generating with digital signal processors and it is convenient for decreasing leakage current, alternating CMV and THD of the inverter. There are three fundamental SPWM modulations applied in H4 inverter topology: bipolar SPWM, unipolar SPWM, and hybrid SPWM. The main differences among these modulation strategies are the switching patterns applied to the switching devices. A sinusoidal modulation signal is compared with a triangle wave carrier signal in the basic principle of the SPWM technique. This operation generates the switching signals required for switching the H-bridge semiconductors. These three strategies are implemented for an H-bridge inverter, as seen in Fig. 3.6. S_1 and S_2 are connected to the same leg, while S_3-S_4 devices are on the next leg. S_1 and S_3 semiconductors are called upper switches, and S_2 and S_4 semiconductors are called lower switches in this configuration.

3.4.1 Bipolar SPWM

Semiconductors in one leg are controlled as complementary in bipolar SPWM for preventing a short circuit of the DC power supply. While S_1 and S_4 are switched to the "ON" state, S_2 and S_3 must be in the "OFF" state. To achieve this switching pattern, a sinusoidal signal must be compared with only one triangle wave signal. The bipolar SPWM modulation strategy is also known as a two-level modulation,

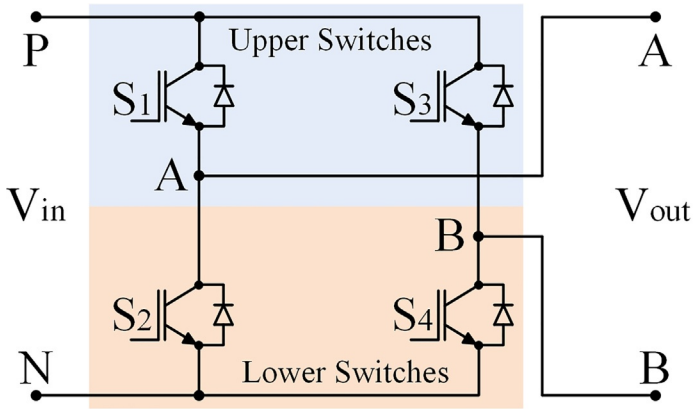

FIG. 3.6

The basic structure of H4 inverter.

which cannot provide a zero-voltage state at the output. If a DC source or a PV panel is connected as a V_{DC} source at the input, the output of the inverter will be changed between $+V_{DC}$ and $-V_{DC}$ when S_1-S_4 and S_2-S_3 are controlled at the same frequency. In this situation, the CMV (V_{AN} and V_{BN} values) becomes a constant value at $V_{DC}/2$ at the output of the inverter, which decreases the leakage current [15–18].

The advantages of bipolar SPWM modulation are stated as low EMI and low leakage current values; however, this method suffers from low efficiency, the requirement of high value filtering components, higher THD ratios, and higher core losses. Hence, the bipolar SPWM modulation strategy can be used in nonisolated grid-tied H4 inverters, but low efficiency and higher THD must be taken into consideration [15–18]. The generation of bipolar SPWM is illustrated in Fig. 3.7, where a sinusoidal modulation signal compared to a carrier triangle signal with "+1 V" and "−1 V" peak references. The generated switching orders seen in the second and third axes indicate that S_1 and S_4 switches are turned "ON" while S_2 and S_3 switches are turned "OFF." The conduction states of switches in the inverter topology are shown in Fig. 3.8A for the first switching order. While S_2 and S_3 switches are turned "ON" in the second order, S_1 and S_4 switches are turned "OFF" as depicted in the last axis of Fig. 3.7, and the circuit configuration is shown in Fig. 3.8B. Table 3.2 shows the summary of switching states for bipolar SPWM. In the bipolar modulation strategy, there is no freewheeling mode in the H4 inverter. Hence, positive or negative input terminals of the inverter are not connected to the grid without connection of a DC source. The leakage current is not affected via a parasitic capacitor to grid neutral. This operation reduces leakage current but varying output voltage without any freewheeling mode causes an incremented THD value and lower efficiency [15–19].

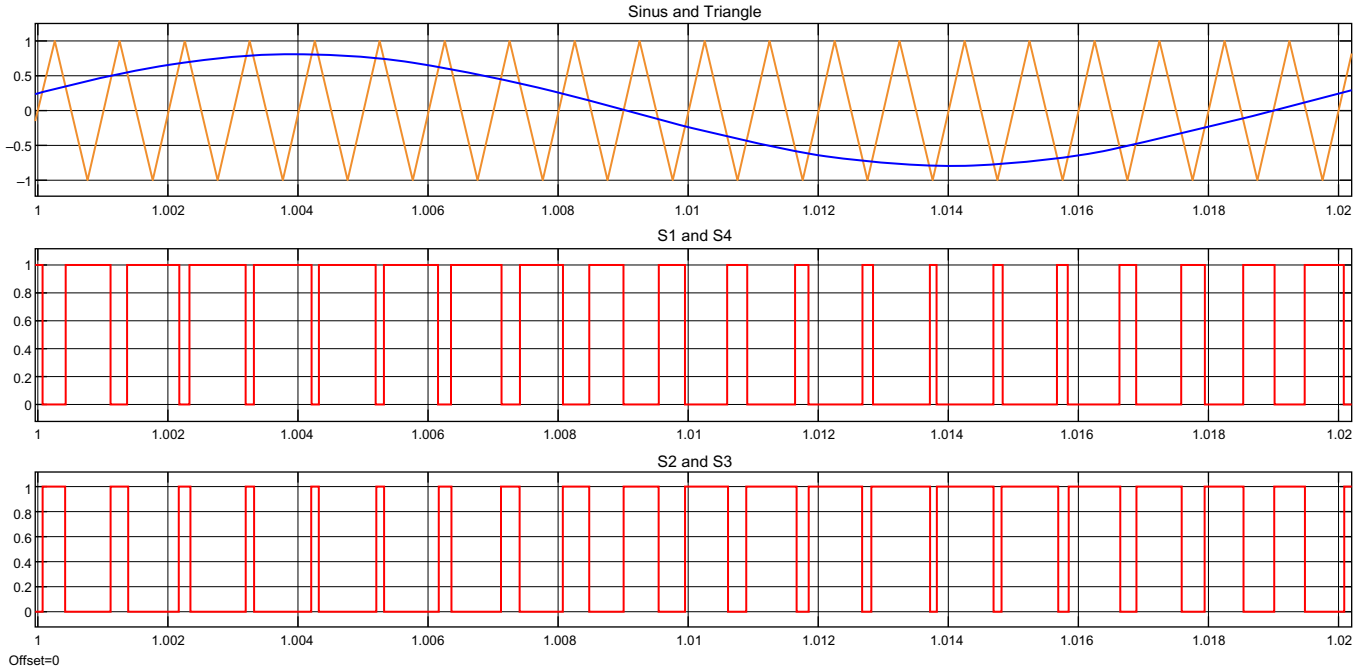

FIG. 3.7

Bipolar SPWM modulation strategy switching states.

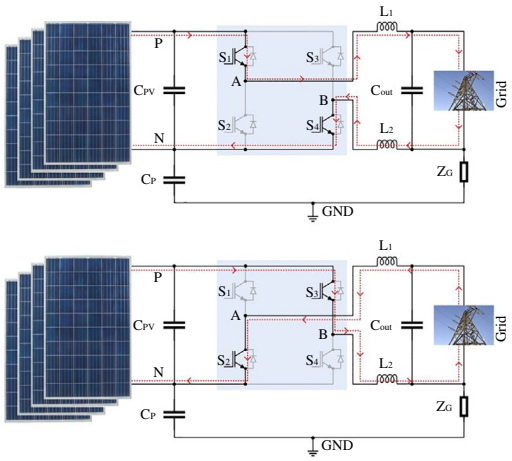

FIG. 3.8

Bipolar SPWM: (A) positive half-cycle (S_1-S_4 = "ON", S_2-S_3 = "OFF"), (B) negative half-cycle (S_2-S_3 = "ON", S_1-S_4 = "OFF").

Table 3.2 Switching states for bipolar SPWM.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4	S_2-S_3	$+V_{DC}$
Negative half-cycle	S_2-S_3	S_1-S_4	$-V_{DC}$

3.4.2 Unipolar SPWM

The unipolar SPWM modulation, also known as three-level modulation, is used in H4 inverters instead of bipolar SPWM for reducing the THD value. The switching states are complementary in one branch of the H4 inverter. For example, S_1 and S_2 are switched in complementary states to each other, and S_3 and S_4 are also complementary to each other, as seen in Fig. 3.9. Two sinusoidal signals that are 180° phase shifted from each other are compared with a triangle carrier signal varying from "0" to "+1" for generating switching signals. If a DC source or a PV panel is connected as V_{DC} in the inverter input, the output levels of the inverter vary between $+V_{DC}$, 0, and $-V_{DC}$ [15–18]. The advantages of unipolar SPWM include decreased values for filtering the inverter output, lower core loss, and higher efficiency (up to 98%) due to reduced losses during the zero voltage state. The disadvantage of unipolar SPWM is that the EMI and leakage current are very high [18].

The generation of unipolar switching states is shown in Fig. 3.9. While the S_4 switching signal is at "ON" in the positive half-cycle, S_1 and S_2 are pulsed as complementary to each other at the carrier frequency. On the other hand, while the S_2 switching signal is at the "ON" position in the negative half-wave, S_3 and S_4 are

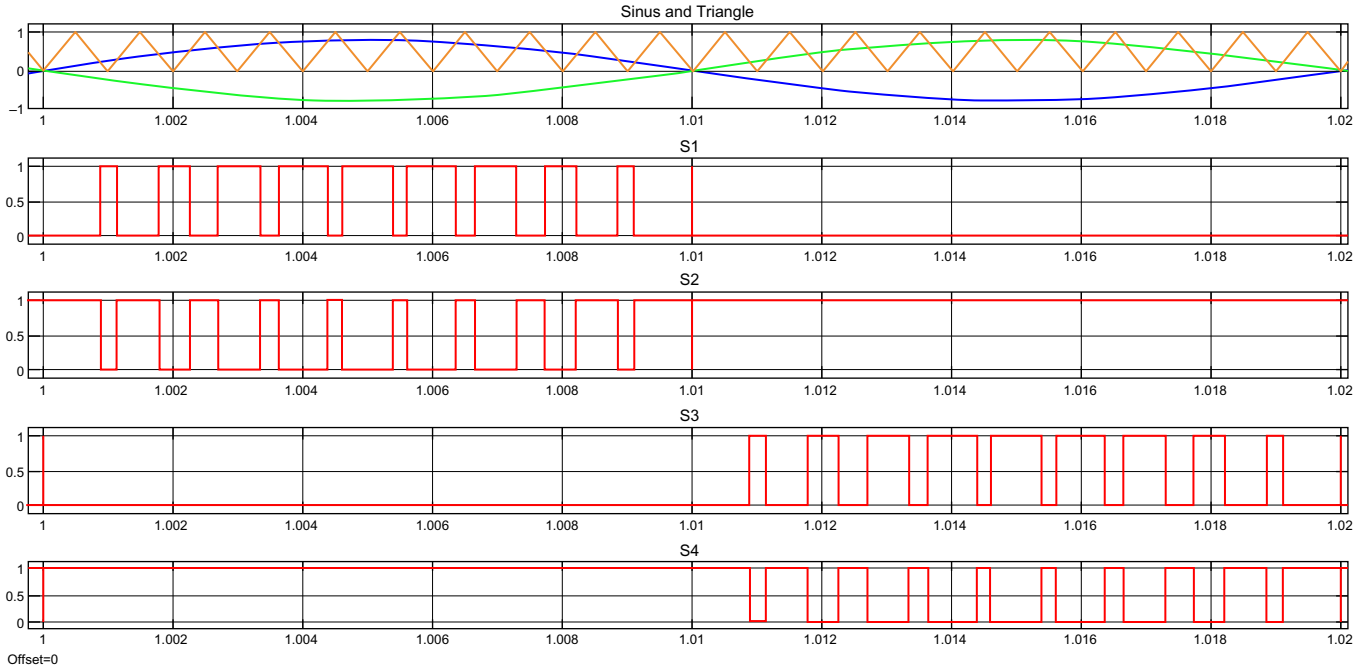

FIG. 3.9

Unipolar SPWM modulation strategy switching states.

pulsed as complementary to each other at the carrier frequency. There are four modes in the unipolar SPWM modulation strategy, as shown in Fig. 3.10. The positive half-cycle and negative half-cycle are depicted in Fig. 3.10A and B, respectively. Freewheeling mode-I and freewheeling mode-II are indicated in Fig. 3.10C and D, respectively. Freewheeling modes achieve zero voltage at the output. Unipolar SPWM is not suitable for nonisolated grid-tied inverters due to the high leakage current and variable CMV [15–18].

Table 3.3 summarizes the switching states of unipolar SPWM where freewheeling mode-I and freewheeling mode-II are identical but switching orders of devices are at different modulation frequencies in these modes. S_4 is always in the "ON" position and S_3 is always in the "OFF" position in freewheeling mode-I. S_1 and S_2 are controlled with complementary PWM signals in carrier frequency. S_2 is at the "ON" position and S_1 is at the "OFF" position in freewheeling mode-II. S_3 and S_4 are switched with complementary PWM signals in carrier frequency [19].

3.4.3 Hybrid SPWM

The hybrid SPWM method is another strategy, like unipolar SPWM, that supports freewheeling modes. One leg is switched at the fundamental frequency while the other leg is switched at the carrier frequency in the hybrid SPWM strategy, as the switching signals are depicted in Fig. 3.11. Two sinusoidal signals that are 180° phase shifted from each other are compared with a triangle carrier signal varying from "0" to "+1" for generating switching signals [10, 18, 19].

The advantages of hybrid SPWM are its lower losses due to unipolar voltage variation ($+V_{DC}$, 0, and V_{DC}), and higher efficiency (up to 98%). The disadvantages of hybrid SPWM are high leakage current and EMI filtering requirements, owing to square wave operation at the fundamental frequency in C_P voltage. Therefore hybrid SPWM is not preferred for nonisolated grid-tied inverter applications, even though it has high efficiency [18].

The current flow operation modes in hybrid SPWM switching states are like unipolar SPWM as depicted in Table 3.4. Hence, hybrid SPWM uses current paths like unipolar SPWM, as depicted in Fig. 3.10, but there are some differences in the frequency of switching in hybrid SPWM. S_1 is kept at the "ON" state and S_2 is turned to the "OFF" state in positive half-cycle and freewheeling mode-II. Furthermore, S_4 and S_3 switches are complementary at the carrier frequency. S_4 is at the "ON" state in the positive half-cycle while S_3 is at the "ON" state in freewheeling mode-II. Also, S_2 is at the "ON" state and S_1 is turned to the "OFF" state in the negative half-cycle and freewheeling mode-I. Furthermore, S_4 and S_3 switches are complementary at the carrier frequency. S_3 is at the "ON" state in the negative half-cycle and S_4 is at the "ON" state in freewheeling mode-I [10, 18, 19]. A comparison of these modulation schemes is shown in Fig. 3.12 from the study of [10]. Characteristics of bipolar SPWM in an H4 inverter are depicted in Fig. 3.12A, while characteristics of unipolar SPWM and hybrid SPWM in an H4 inverter are depicted in Fig. 3.12B and C.

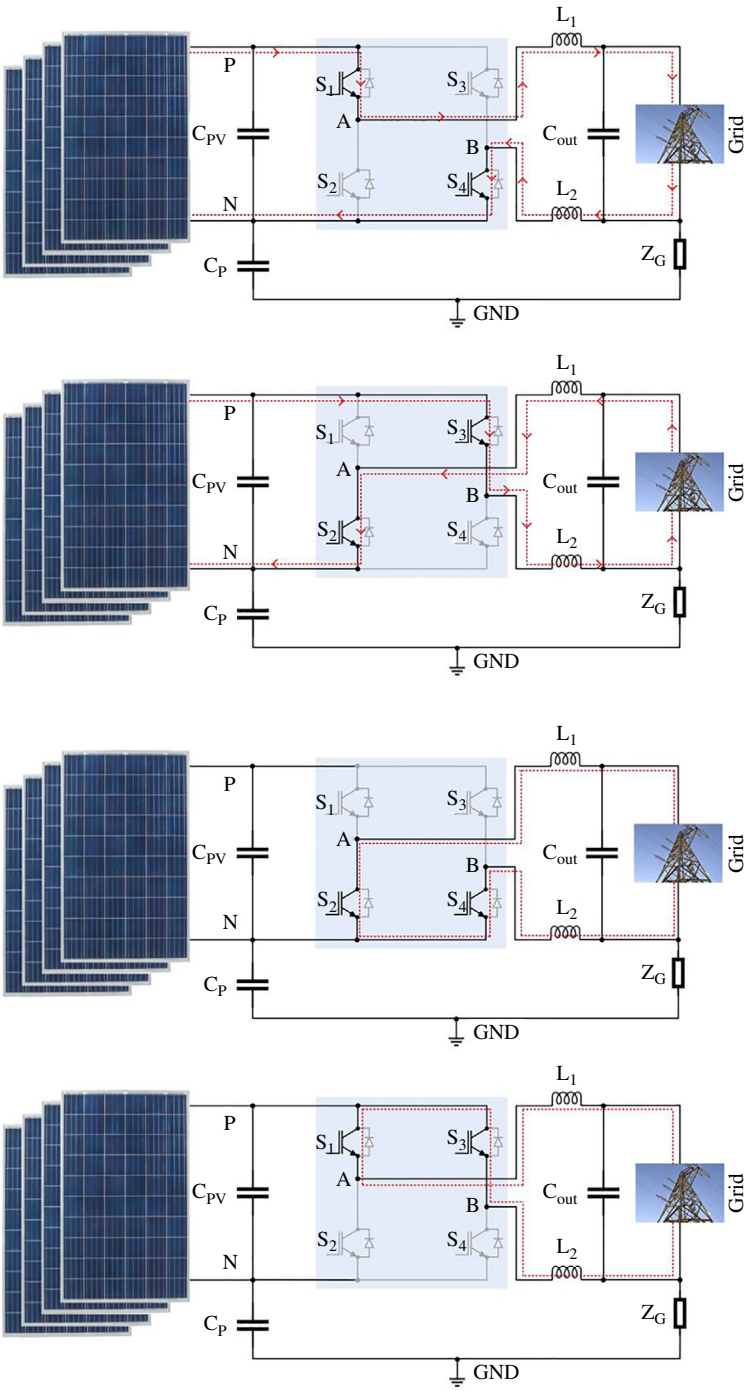

FIG. 3.10

Unipolar SPWM: (A) positive half-cycle, (B) negative half-cycle, (C) freewheeling mode-I, (D) freewheeling mode-II.

Table 3.3 Switching states for unipolar SPWM.

Switching State	"ON" state Switches	"OFF" state Switches	V_{out}
Positive half-cycle	S_1-S_4	S_2-S_3	$+V_{DC}$
Freewheeling mode-I	S_2-S_4	S_1-S_3	0
Freewheeling mode-II	S_1-S_3	S_2-S_4	0
Negative half-cycle	S_2-S_3	S_1-S_4	$-V_{DC}$

The output voltage and current waveforms of the different modulation strategies are fairly close to each other. Basic differences are seen in the variation of CMV caused by V_{AN} and V_{BN} values. The CMV value is constant in bipolar SPWM, as seen in Fig. 3.12A. Therefore the lowest leakage current (15.4 mA) is achieved in bipolar SPWM. The leakage current of unipolar SPWM is 1.8 A and the leakage current of hybrid SPWM is 3.9 A [10].

3.5 H5 inverter topology

H4 inverter topology is not quite suitable for the nonisolated grid-tied inverter, due to leakage current and CMV. The bipolar modulation strategy in the H4 inverter provides constant CMV and it enables low leakage current to be achieved, but the THD ratio and efficiency values of the H4 inverter are undesirable. The unipolar modulation strategy can be used for preventing the disadvantages of bipolar modulation, but the CMV does not present a constant value and the leakage current is increased. However, these limitations of the H4 inverter topology can be overcome by using an extra switch for cutting the connection of PV systems with the grid via the C_P capacitor. This topology is called H5 and it was proposed and patented by SMA Solar Technology in 2005 [17].

The H5 inverter topology has a different structure than the H4 topology, with an additional DC-bypass switch (S_5) that disconnects the PV from the grid in freewheeling modes and thus allowing constant CMV. Therefore, the leakage current is smaller than in H4 topology with the bipolar SPWM strategy. The H5 inverter topology, which is classified as a DC-bypass method, is depicted in Fig. 3.13 [20]. The switching states of H5 topology are listed in Table 3.5, with the positive half-cycle obtained while S_1, S_4, and S_5 switches are "ON" and S_2 and S_3 switches are "OFF", as seen in Fig. 3.14A. In the negative half-cycle, S_2, S_3, and S_5 switches are "ON" and S_1 and S_4 switches are "OFF", as seen in Fig. 3.14B. Two sinusoidal signals and one triangle signal are used for generating the switching order as in the unipolar SPWM. However, switching frequency applied to the switches is different from that in unipolar SPWM. The upper switches (S_1 and S_3) are switched at the fundamental frequency. However, the lower switches (S_2 and S_4) are switched at the carrier frequency (or higher frequency). The switching signals and switching orders are shown in Fig. 3.15 [4, 9, 11, 17–20].

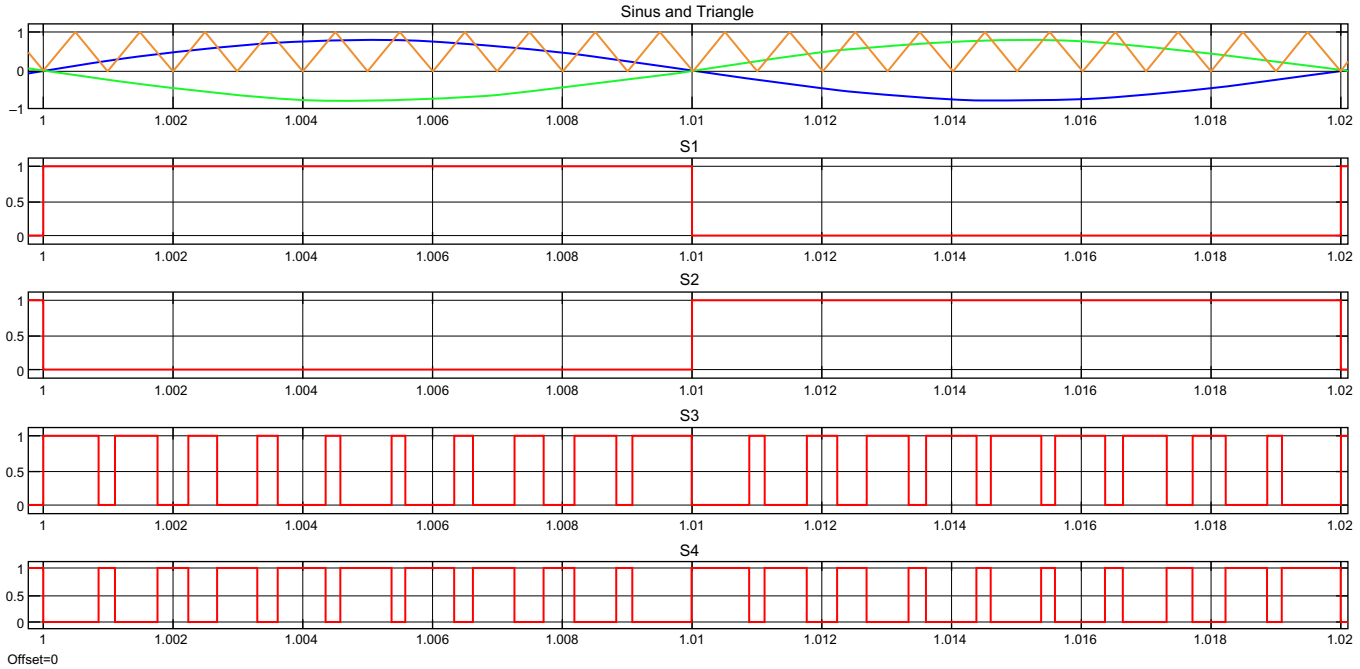

FIG. 3.11

Hybrid SPWM modulation strategy switching states.

Table 3.4 Switching states for hybrid SPWM.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4	S_2-S_3	$+V_{DC}$
Freewheeling mode-I	S_2-S_4	S_1-S_3	0
Freewheeling mode-II	S_1-S_3	S_2-S_4	0
Negative half-cycle	S_2-S_3	S_1-S_4	$-V_{DC}$

There are two freewheeling modes available in the H5 inverter, as shown in Fig. 3.14C and D. Switching states of the freewheeling modes are shown in Table 3.5. All the switches are operated at the "OFF" state except the S_1 in freewheeling mode-I, but current flow in this mode is sustained over the antiparallel diode of S_3. Furthermore, all the switches are in the "OFF" state except the S_3 in freewheeling mode-II, so that the current flow is maintained over the antiparallel diode of S_1 in this mode. Also, the DC-bypass diode (S_5) is switched at the carrier frequency, and the S_5 switching signal is generated by the AND logic operation of S_2 and S_4. The advantages of the H5 inverter are lower core losses due to unipolar voltage variation, higher efficiency (up to 98%), fewer EMI filtering component requirements, and reduced leakage current. The disadvantages of the H5 inverter are higher conduction losses, but the overall high efficiency is not affected, and the addition of one extra switch [4, 9, 11, 17–20].

Characteristic output waveforms of the H5 inverter topology are shown in Fig. 3.16 from the study of [10]. V_{AB}, which is output voltage, varies between $+V_{DC}$, 0, $-V_{DC}$ and it decreases the CMV at the unipolar modulation. The variation of CMV is better than with unipolar SPWM and hybrid SPWM but is higher than the bipolar SPWM. Hence, the THD values of H5 topology (1%) are lower than with bipolar SPWM (1.8%) while the leakage current of bipolar SPWM (15.4 mA) is the lowest, compared to the leakage current of the H5 inverter at 23.4 mA [10].

3.6 H6 inverter topology

The H6 inverter, introduced by Ingeteam, is another DC bypass topology improved in order to reduce the CMV in inverters for achieving less leakage current. There are six switches in the H6 topology, as its name implies. An extra switch is connected in the negative bus of the DC-link of the H5 topology, as seen in Fig. 3.17. The switches connected to the positive and negative bus of the DC-link are used to disconnect the PV source from the grid in freewheeling mode. Therefore, C_P and its effect on CMV are decreased and inverter operation can be achieved with less leakage current [1, 2, 9, 10].

The switching states of the inverter are shown in Fig. 3.18, where it can be seen that there are two sinusoidal signals and one triangle signal is used in the comparator, as in unipolar SPWM. However, the H-bridge section of the H6 inverter topology

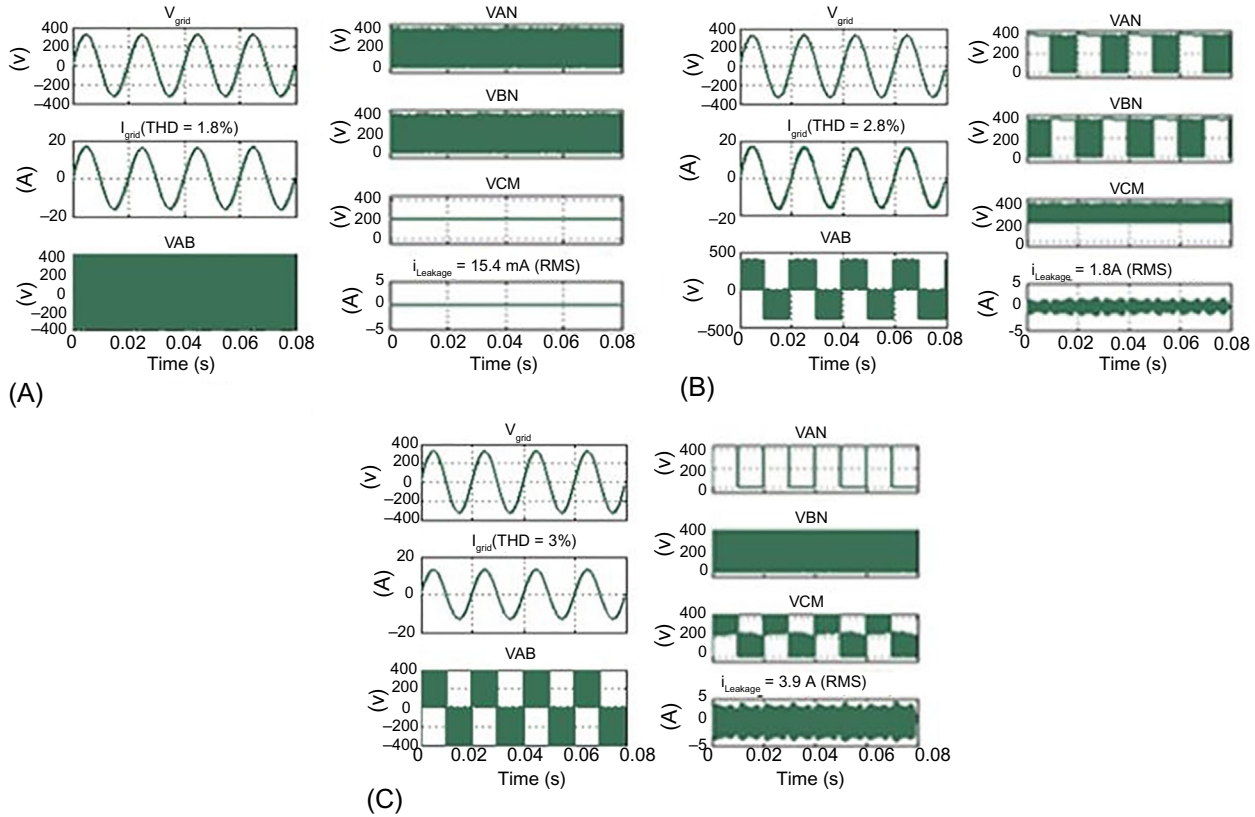

FIG. 3.12

Characteristic output waves of H4 inverter at different modulation schemes: (A) bipolar SPWM, (B) unipolar SPWM, (C) hybrid SPWM [10].

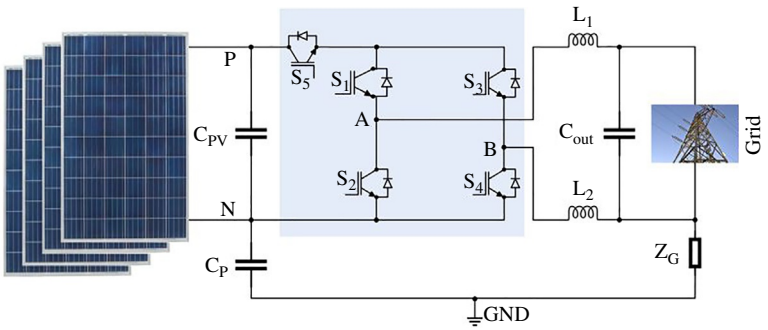

FIG. 3.13

H5 inverter topology.

Table 3.5 Switching states of H5 topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4-S_5	S_2-S_3	$+V_{DC}$
Freewheeling mode-I	S_1-S_3(antiparallel diode)	S_2-S_3-S_4-S_5	0
Freewheeling mode-II	S_3-S_1(antiparallel diode)	S_1-S_2-S_4-S_5	0
Negative half-cycle	S_2-S_3-S_5	S_1-S_4	$-V_{DC}$

operates as in the hybrid SPWM strategy. The S_1 and S_2 switch legs are switched at the fundamental frequency, and S_3 and S_4 are switched at the carrier frequency. The S_5 switch is turned "ON" during the negative half-cycle that is switched at the carrier frequency by the logic AND operation of S_1 and S_4 in the positive half-cycle. The S_6 switch that is switched at the carrier frequency generated by the logic AND operation of S_2 and S_3 in the negative half-cycle is operated at the "ON" state during the positive half-cycle [2, 10].

The operation states of the topology are illustrated in Table 3.5, where the unipolar voltage variation ($+V_{DC}$, 0, $-V_{DC}$) occurs in the H6 topology. Switching states of the positive half-cycle given in Table 3.5 are depicted in Fig. 3.19A. Also, switching states of the negative half-cycle are shown in Fig. 3.19B. The freewheeling mode-I and freewheeling mode-II are illustrated in Fig. 3.19C and D, respectively.

Positive half-cycle states and freewheeling mode-I are successively operated in positive half-cycle, while the freewheeling mode-II is operated in negative half-cycle states (Table 3.6).

Characteristic output waves of the H6 inverter are shown in Fig. 3.20 [10]. V_{AB}, which is output voltage, varies between $+V_{DC}$, 0, $-V_{DC}$ and lower CMV is seen at this unipolar operation. The variation of CMV rates obtained in bipolar modulation is better than in unipolar and hybrid SPWM in the H6 topology. A small difference is noted between the leakage current of bipolar SPWM (15.4 mA) and the leakage

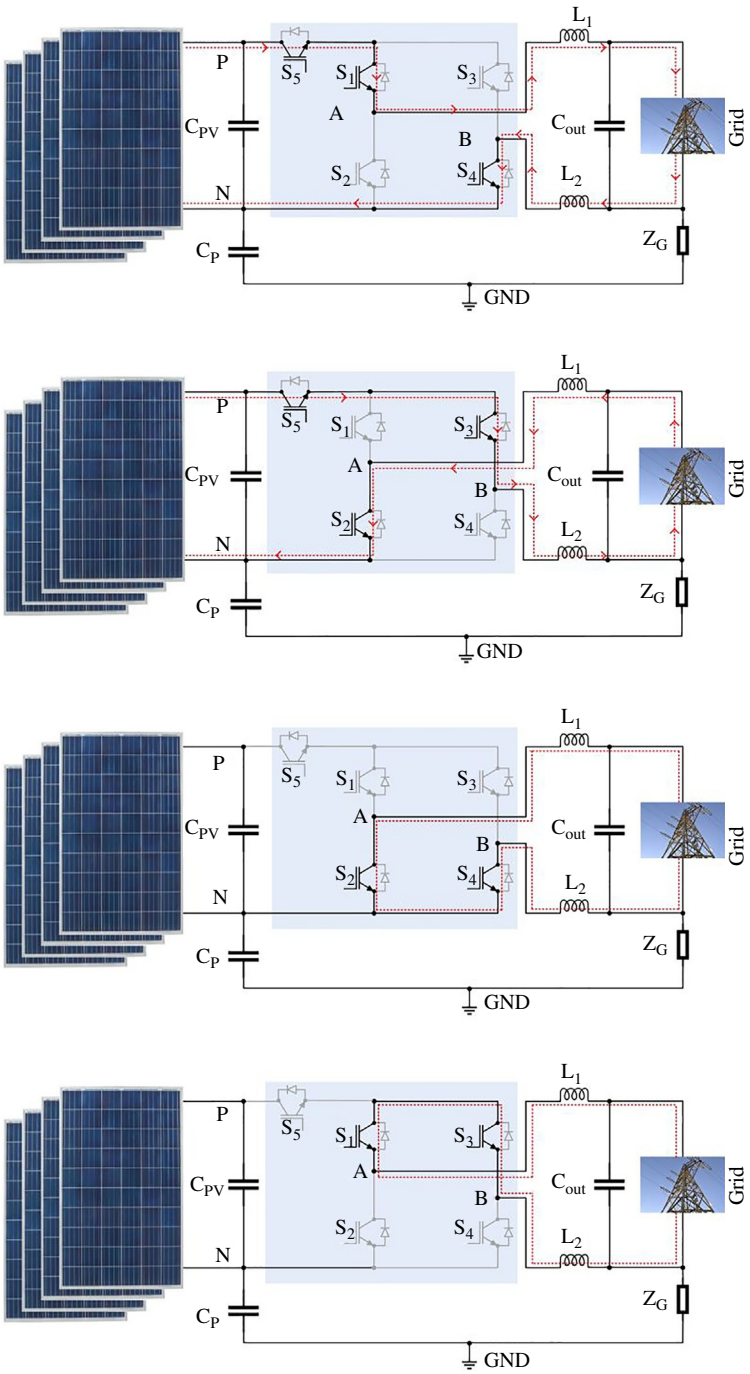

FIG. 3.14

H5 inverter: (A) positive half-cycle, (B) negative half-cycle, (C) freewheeling mode-I, (D) freewheeling mode-II.

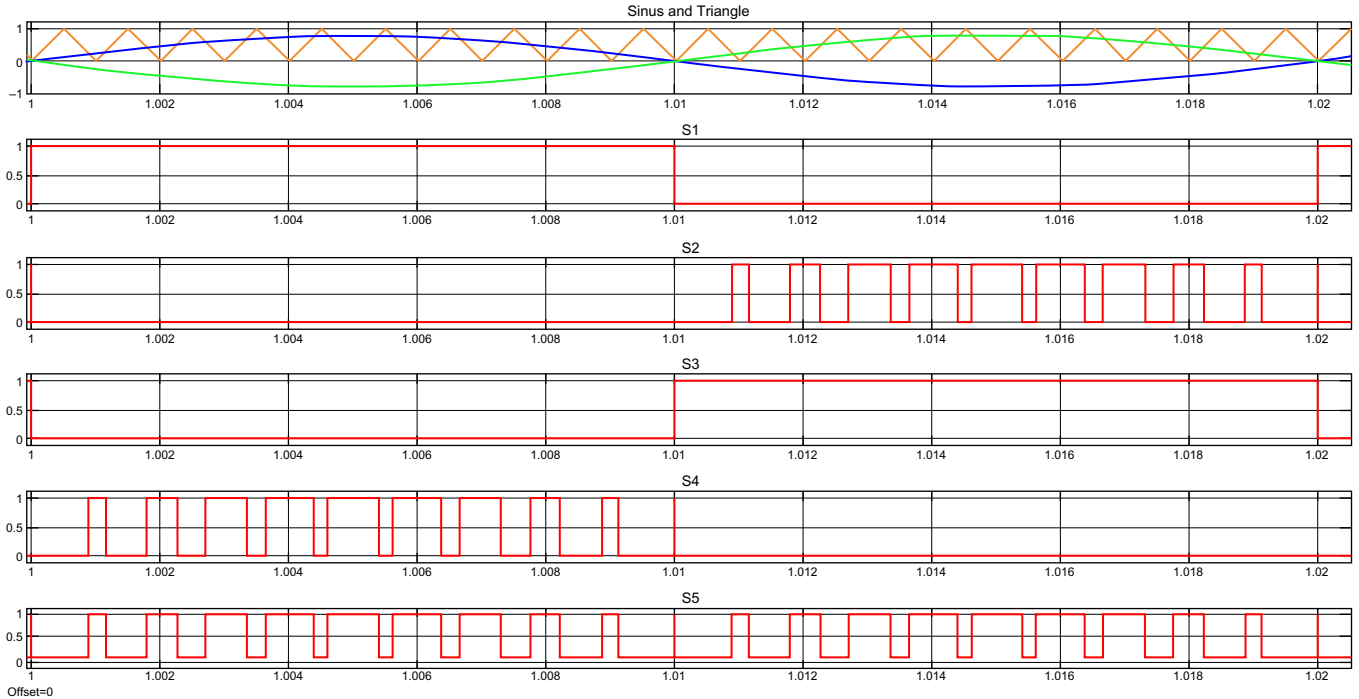

FIG. 3.15

Switching signals in H5 topology.

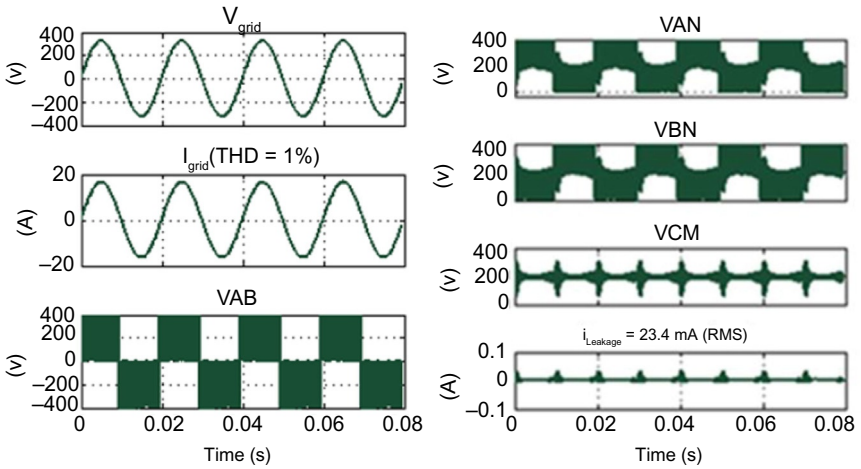

FIG. 3.16

Characteristic output waveforms of H5 inverter [10].

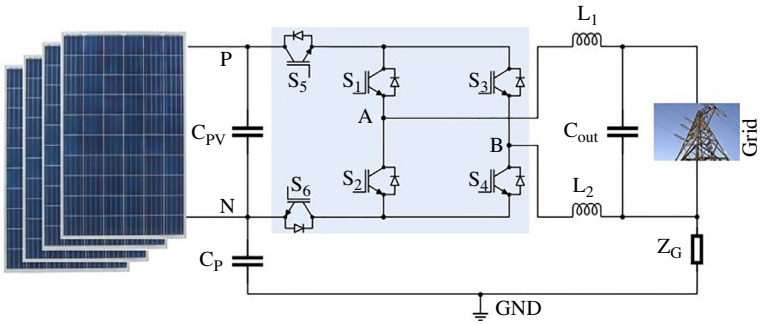

FIG. 3.17

H6 inverter topology.

current of the H6 inverter (16.09 mA), while the THD rates of H6 (1.1%) are better than with bipolar SPWM (1.8%); 1% was obtained with H5 inverter topology under similar operating conditions [10].

3.7 HERIC inverter

The HERIC topology was proposed by Schmidt et al. Two switches (S_A and S_B) are connected to the AC output of the H4 topology in the HERIC inverter, as shown in Fig. 3.21. The topology is implemented to decrease the leakage current and increase the efficiency by using a bypass operation at the AC side of the inverter. These

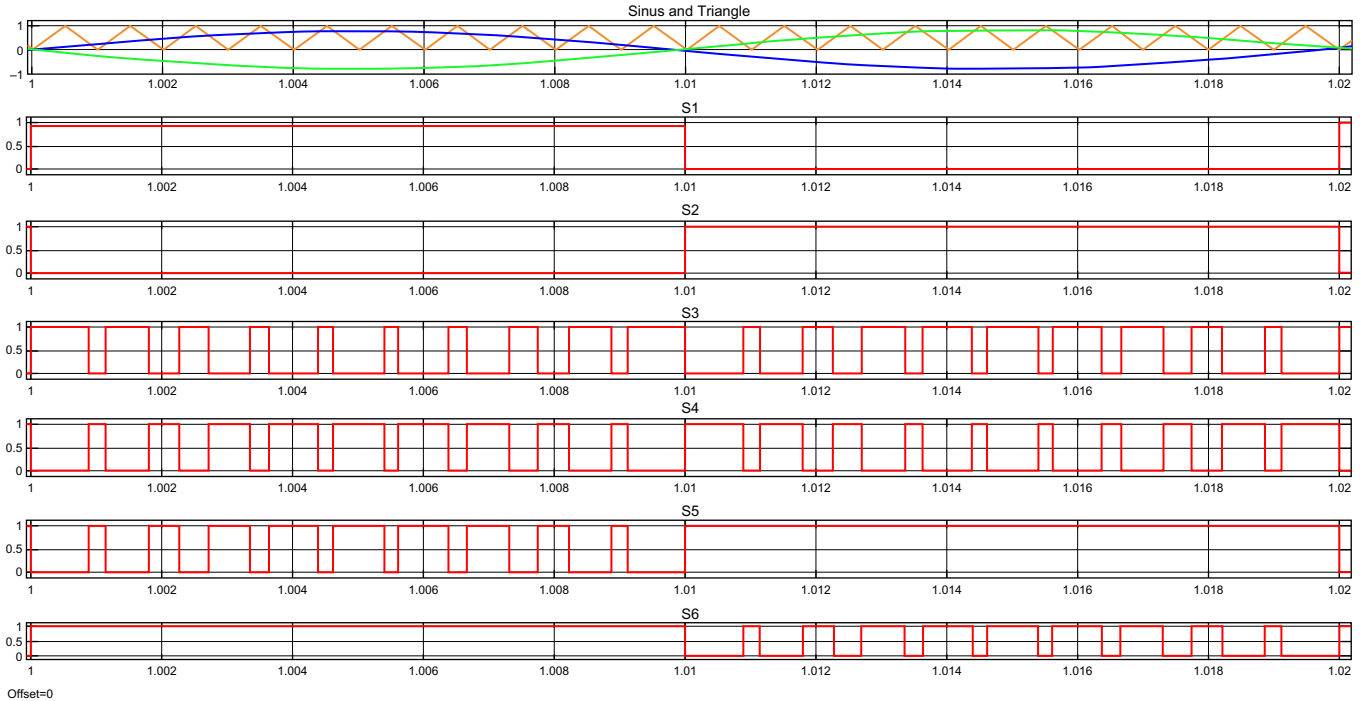

FIG. 3.18

Switching signals in H6 topology.

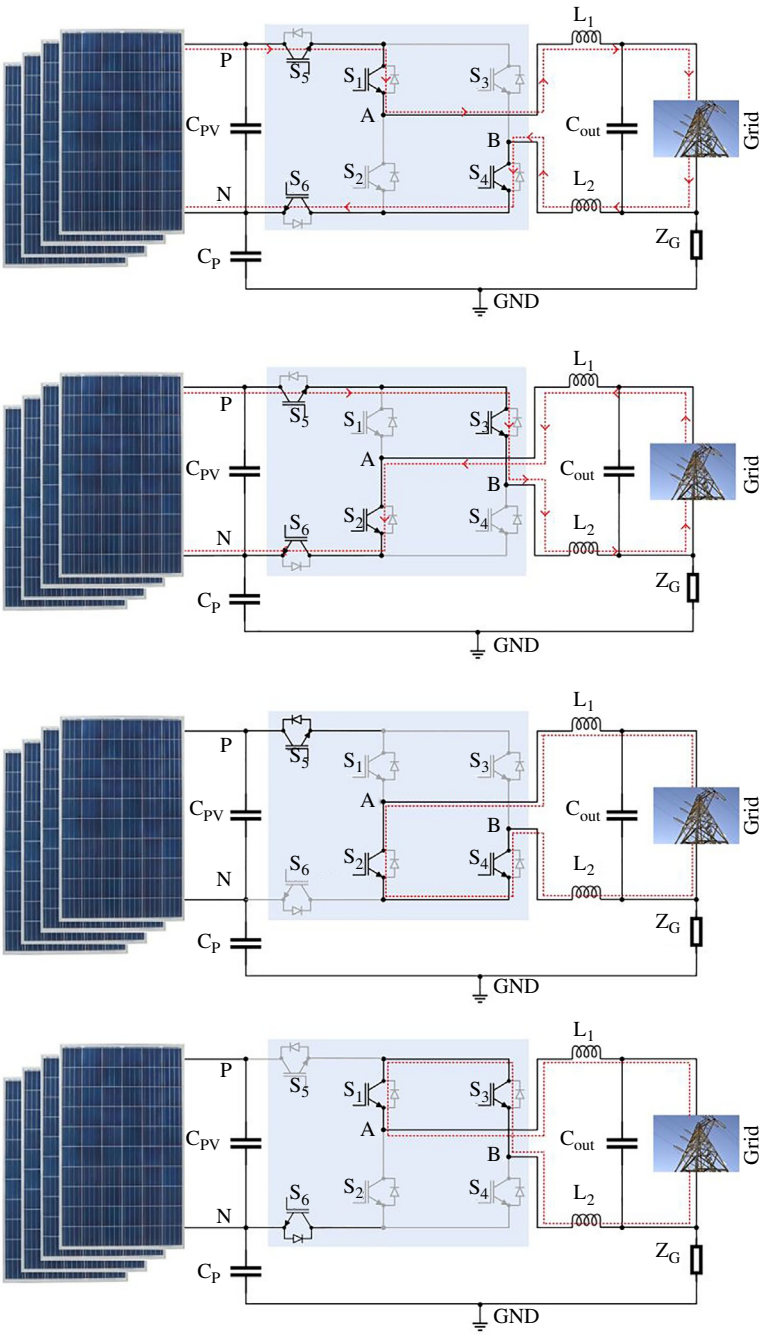

FIG. 3.19

H6 inverter: (A) positive half-cycle, (B) negative half-cycle, (C) freewheeling mode-I, (D) freewheeling mode-II.

Table 3.6 Switching states of H6 topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4-S_5-S_6	S_2-S_3	$+V_{DC}$
Freewheeling mode-I	S_1-S_3-S_6	S_2-S_4-S_5	0
Freewheeling mode-II	S_2-S_4-S_5	S_1-S_3-S_6	0
Negative half-cycle	S_2-S_3-S_5-S_6	S_1-S_4	$-V_{DC}$

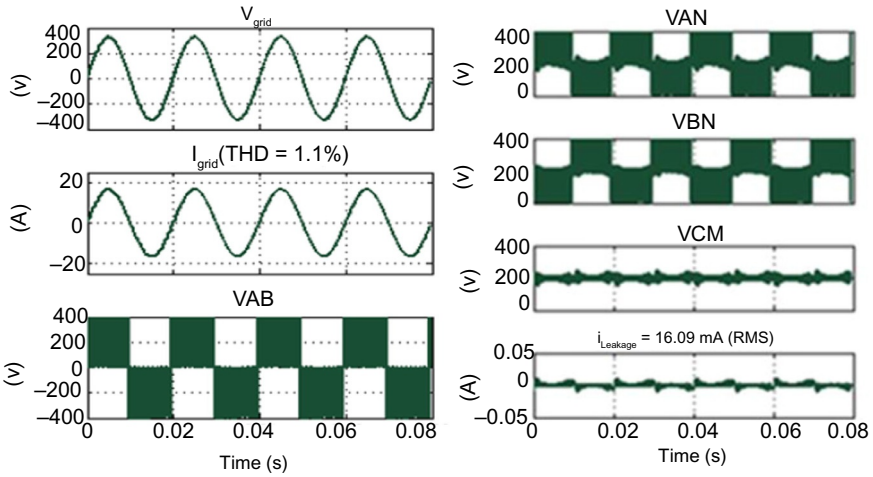

FIG. 3.20

Characteristic output waves of H6 inverter [10].

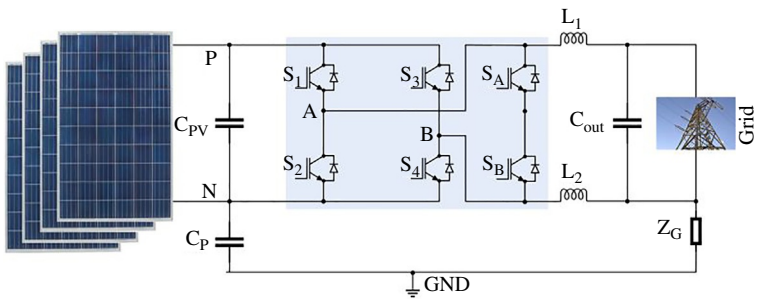

FIG. 3.21

HERIC inverter topology.

switches generate a zero voltage level in freewheeling modes. Also, the output of the inverter is disconnected from PV neutral in these operation modes. The HERIC inverter has three output voltage levels ($+V_{DC}$, 0, $-V_{DC}$) that are obtained by using a unipolar SPWM strategy. The switching order decreases the leakage current due to constant CMV. Furthermore, the efficiency of the inverter remains high because the output current is short-circuited via S_A or S_B during the freewheeling modes. The HERIC inverter is expected to perform well in nonisolated PV inverter systems, because of the high efficiency and very low leakage current and EMI [1, 2, 10, 14, 16].

The switching states of the HERIC inverter are shown in Fig. 3.22 and four operation modes are depicted in Table 3.7. The H-bridge switching devices (S_1, S_2, S_3, S_4) are switched at carrier (high) frequency and the AC bypass switches (S_A and S_B) are controlled at the fundamental frequency. In addition, the S_1-S_4 and S_2-S_3 switches are operated in a similar way to bipolar SPWM. The S_A and S_B are switched complementarily, and using AC bypass switches provides lower losses due to the reduced number of switches in the current conduction path [2, 10, 19, 21].

The positive half-cycle is illustrated in Fig. 3.23A. In this mode, S_1, S_4, and S_A are "ON" states where the S_1 and S_4 are switched at high frequency. While S_1 and S_4 are at the "OFF" state, the HERIC inverter operates in freewheeling mode-I, as seen in Fig. 3.23C. The current path crosses from S_A and the antiparallel diode of S_B in freewheeling mode-I. The S_2, S_3, and S_B are at "ON" state in the negative half-cycle, as depicted in Fig. 3.23B. While S_2 and S_3 are turned to the "OFF" state, the HERIC inverter operates in freewheeling mode-II, as seen in Fig. 3.23D. The current path crosses from S_B and the antiparallel diode of S_A in freewheeling mode-II [2, 10, 19, 21].

Characteristic output waveforms of the HERIC inverter are shown in Fig. 3.24 [10]. The current THD rises to 1.7% due to the modulation of H-bridge switches, but the output voltage varies between $+V_{DC}$, 0, $-V_{DC}$ and lower CMV is seen. The leakage current of the HERIC inverter is measured at 23.5 mA, which is lower than in unipolar SPWM (1.8 A) and hybrid SPWM (3.9 A) of the H4 inverter, while it is almost the same as that of the H5 inverter (23.4 mA); however, it is higher than in the H6 inverter (16.09 mA) and the bipolar SPWM of the H4 inverter (15.4 mA) [10].

3.8 Recent H-bridge based multilevel topologies

The topologies implemented for nonisolated inverters have been extensively studied by researchers. Basic topologies such as H4, H5, H6, and HERIC are still being developed for achieving constant CMV and reducing leakage current and THD ratios. Recent H-bridge topology based on nonisolated multilevel topologies includes additional diodes, switches, and capacitors in the structure. These extra components make the inverter more complicated and expensive.

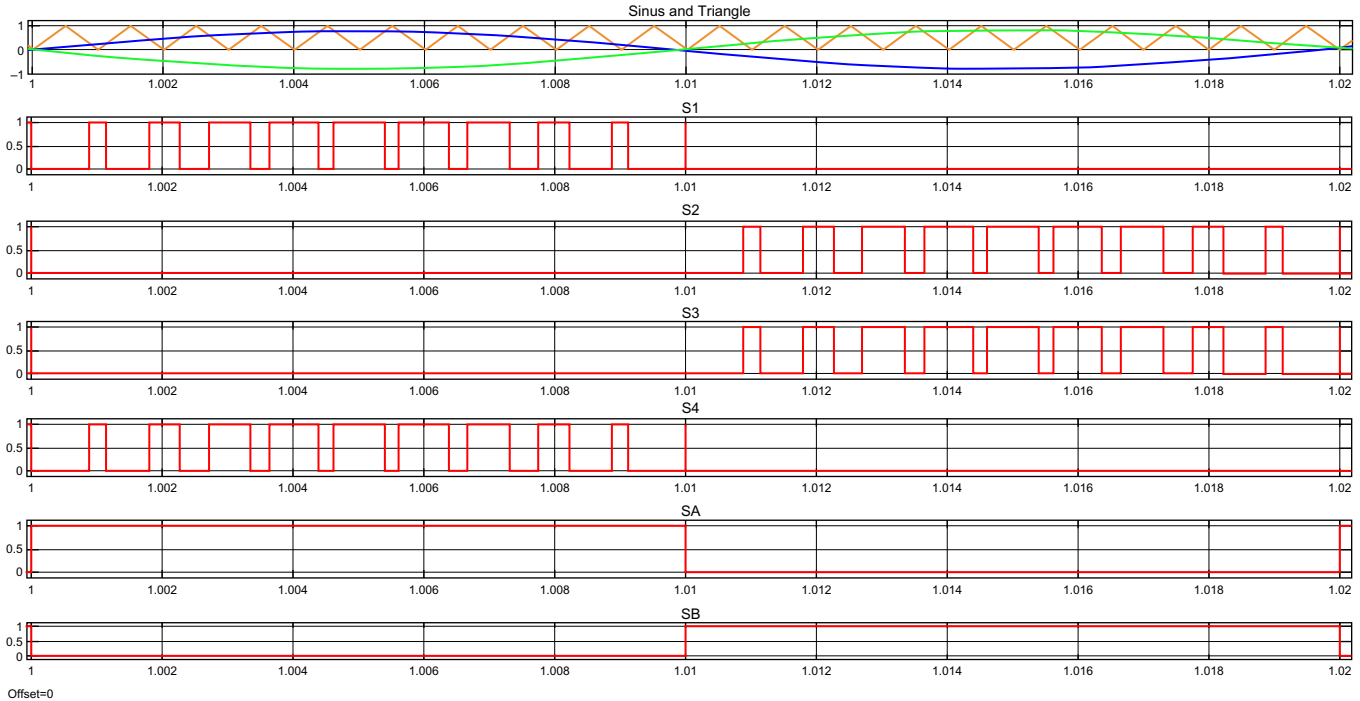

FIG. 3.22

Switching signals in HERIC topology.

Table 3.7 Switching states of HERIC topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4-S_A	S_2-S_3	$+V_{DC}$
Freewheeling mode-I	S_A-S_B(antiparallel diode)	S_1-S_2-S_3-S_4	0
Freewheeling mode-II	S_B-S_A(antiparallel diode)	S_1-S_2-S_3-S_4	0
Negative half-cycle	S_2-S_3-S_B	S_1-S_4	$-V_{DC}$

3.8.1 Optimized H5 topology

The optimized H5 (oH5) topology has been proposed by Huafeng et al. in [22]. An extra switch is included as parallel to the positive terminal of the DC-link, as seen in Fig. 3.25. The sixth switch is connected between the middle point of the voltage divider capacitance and CMV is clamped to $V_{DC}/2$ in the freewheeling mode. The H-bridge switches of this inverter are controlled similarly to those of the hybrid SPWM. The switches are operated based on grid voltage polarity at high frequency or grid frequency, as depicted in Fig. 3.26. The switches of oH5, which are S_1-S_2, S_3-S_4, and S_5-S_6, are switched complementarily to each other and the operating frequency of the switches can be seen in Fig. 3.26. The switching state modes are represented in Table 3.8, and these states provide isolation between the grid and PV modules. S_5-S_6 are switched complementarily but they must have dead time in switching states to protect the capacitors from short circuits. Higher conduction losses are one of the other disadvantages of the oH5 inverter. Characteristic output waveforms of the HERIC inverter are shown in Fig. 3.27, which is presented in [10]. The lowest leakage current is achieved at 5.8 mA in the oH5 inverter and the THD of this inverter is measured at 1%. Hence, the oH5 inverter topology has proposed better power quality, comparing the discussed topologies [2, 10, 22].

3.8.2 H6-I and H6-II inverter topology

H6-I and H6-II inverters have six switches, as seen in Figs. 3.28 and 3.29, respectively. Two extra switches are added to the middle point of an H-bridge. The structure of these two topologies is similar. Differences in these topologies are the connection point of the diodes and the output of the inverter is connected to a different point of the inverter. Two freewheeling diodes are included in these inverters with the same connection method. The output of the inverter is connected to the upper side of the middle point switches (S_5 and S_6) in the H6-I topology. Also, the output of the inverter is connected to the lower side of the middle point switches (S_5 and S_6) in the H6-II topology. Advantages of H6-I and H6-II are high efficiency, low leakage current due to the parasitic capacitance, smaller output inductance, and no need for dead time [2, 5, 10, 23, 24].

Switching states are illustrated in Fig. 3.30 for the H6-I inverter topology and in Fig. 3.31 for the H6-II inverter topology. H-bridge switches (S_1, S_2, S_3, S_4) are switched in unipolar SPWM for the H6-I and H6-II inverters. Middle point switches

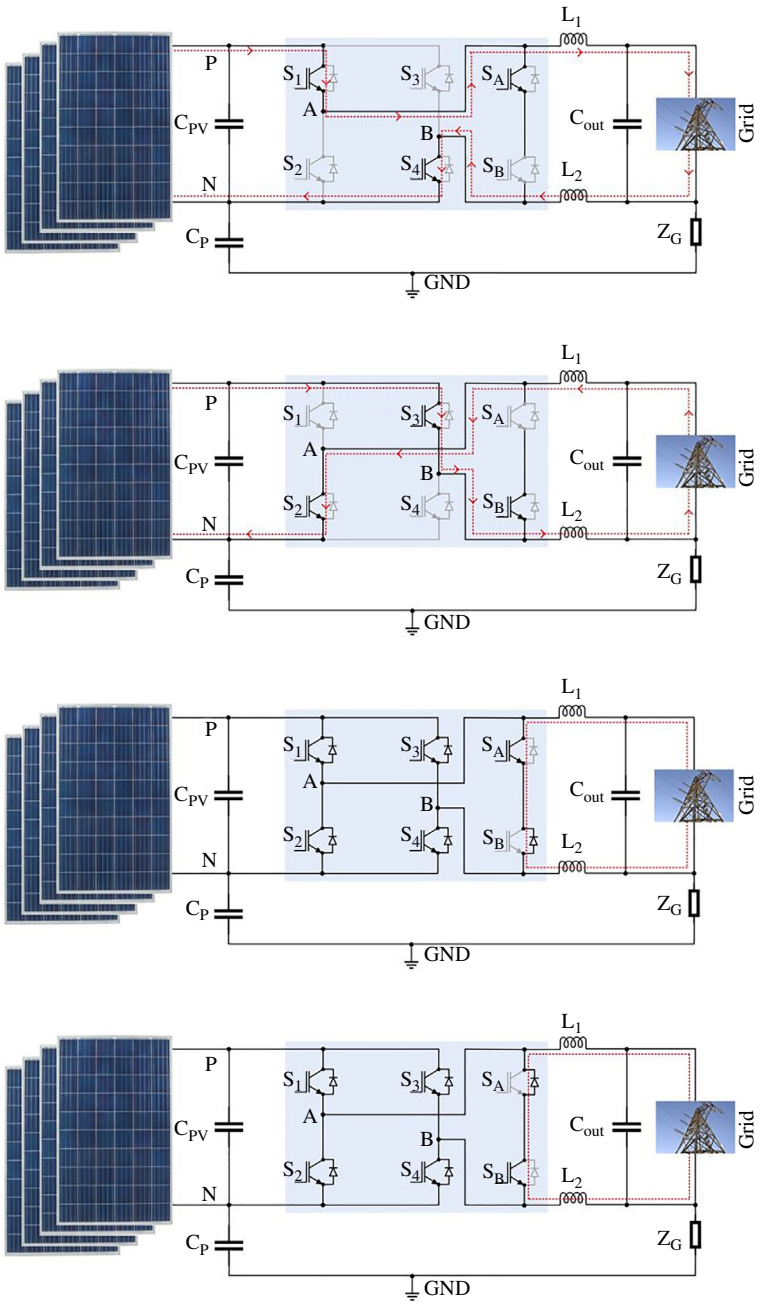

FIG. 3.23

HERIC inverter: (A) positive half-cycle, (B) negative half-cycle, (C) freewheeling mode-I, (D) freewheeling mode-II.

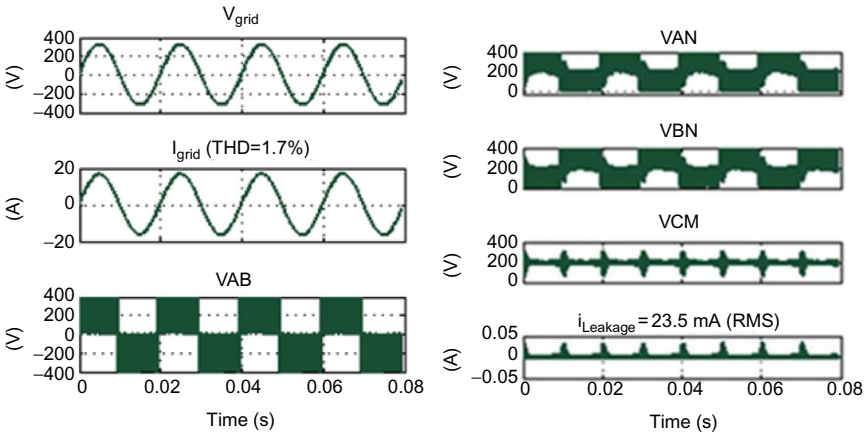

FIG. 3.24

Characteristic output waves of HERIC inverter [10].

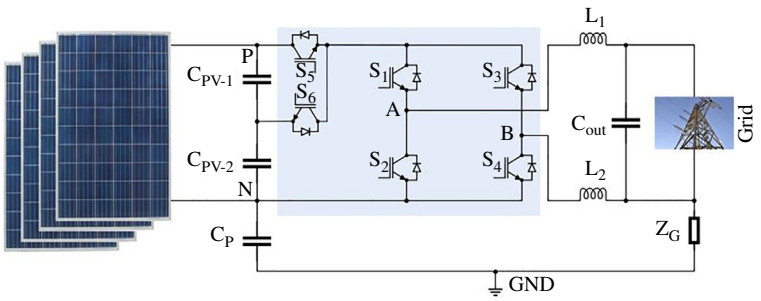

FIG. 3.25

The oH5 inverter topology.

(S_5 and S_6) are switched due to the polarity of output waves. S_5 is "OFF" and S_6 is "ON" for the positive half-cycle in H6-I, and vice versa in the negative half-cycle in H6-I inverter topology. The S_5 and S_6 switches operate inverse switching states from H6-I in the H6-II inverter topology [2, 5, 10, 23, 24].

The current path is explained in Tables 3.9 and 3.10 for the H6-I and H6-II inverter topologies, respectively. Only middle point switches change their position in the current path of positive, negative, and freewheeling modes. Characteristic output waves of these inverters are shown in Fig. 3.32. The leakage current is around 16 mA in H6-I and current THD is 2.6%, as depicted in Fig. 3.32A. Output values of the H6-II inverter topology are shown in Fig. 3.32B and here the leakage current is raised to 21.04 mA and THD is reduced to 2.3% [10].

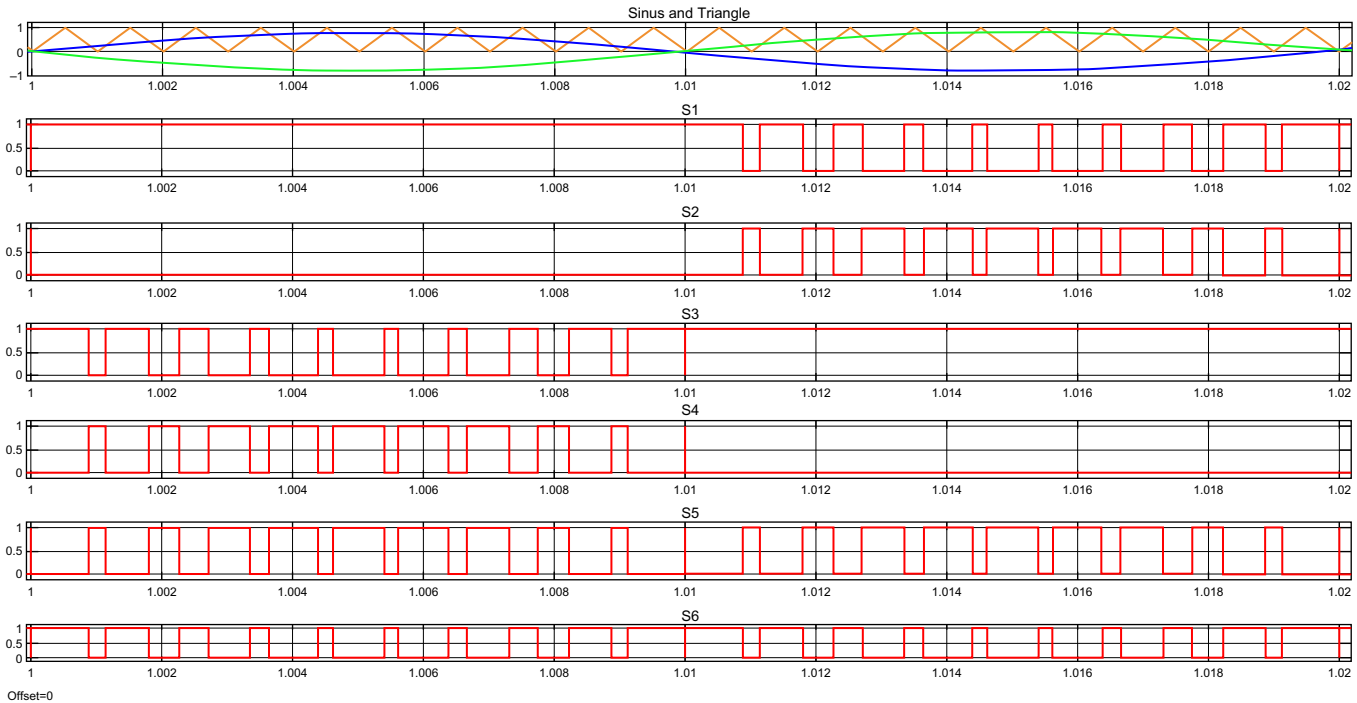

FIG. 3.26

Switching signals in oH5 inverter topology.

Table 3.8 Switching states of oH5 topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4-S_5	S_2-S_3-S_6	$+V_{DC}$
Freewheeling mode-I	S_1-S_3(antiparallel diode)	S_2-S_4-S_5-S_6	0
Freewheeling mode-II	S_3-S_1(antiparallel diode)	S_2-S_4-S_5-S_6	0
Negative half-cycle	S_2-S_3-S_5	S_1-S_4-S_6	$-V_{DC}$

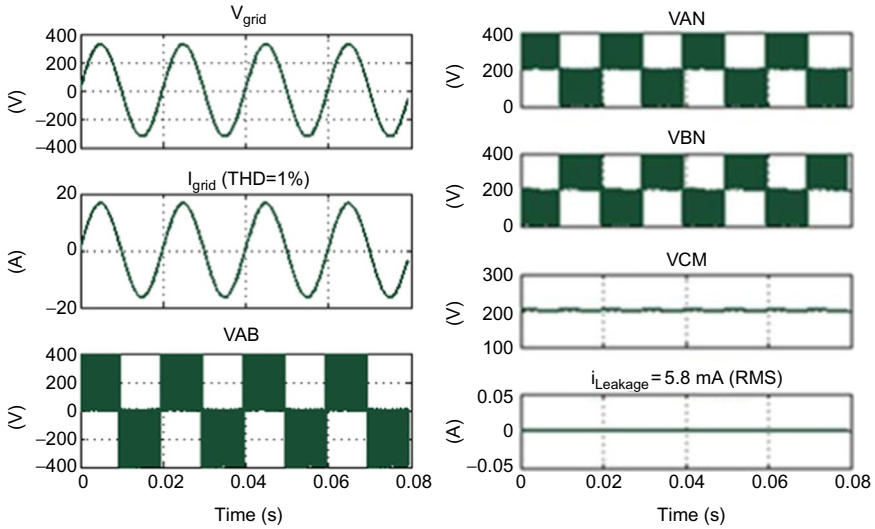

FIG. 3.27

Characteristic output waves of oH5 inverter [10].

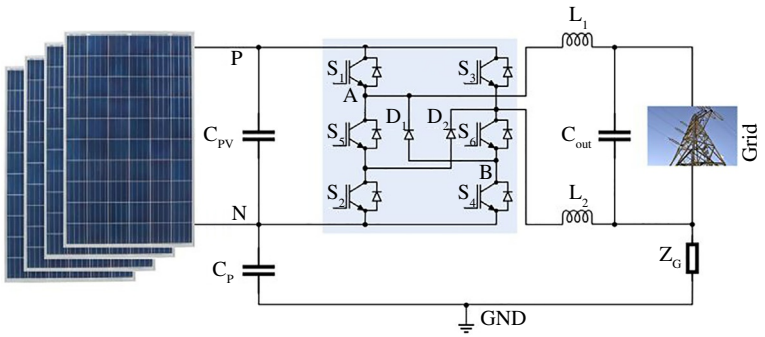

FIG. 3.28

H6-I inverter topology.

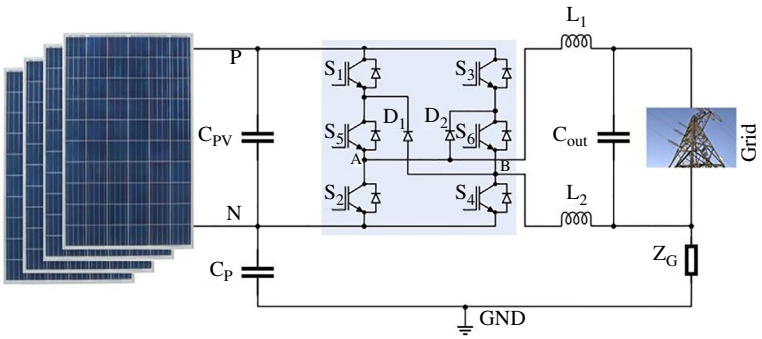

FIG. 3.29

H6-II inverter topology.

3.8.3 H6-III

The H6-III topology was proposed by Islam and Mekhilef in [5]. The structure of the H6-III topology was improved by adding a middle point, compared to H6-I and H6-II topologies. Two diodes acting as freewheeling modes in the middle points were removed. The structure of H6-III topology is depicted in Fig. 3.33, where the output of the inverter comprises from the upper point of the S_5 and S_6 switches. Unlike the H6-I and H6-II topologies, the H6-III topology is capable of injecting reactive power to the utility grid [5, 10]. The H-bridge switches, S_1-S_4, are switched at high frequency according to the polarity of the grid voltage, as shown in Fig. 3.34, while S_5 is in the "ON" state in positive half-cycle and is switched at high frequency in the negative half-cycle. S_6 is in the "ON" position in the negative half-wave and switches at high frequency in the positive half-wave.

While S_1-S_4 switches are in the "OFF" state, S_5 and S_6 switches provide the freewheeling path. Therefore, CMV is linear and does not alternate, as seen in Fig. 3.35. The current path of the H6-III inverter is explained in Table 3.11 for positive, negative, and freewheeling modes.

Lower leakage current is seen, at about 9.8 mA, and the THD ratio is remarkably low. Characteristic output waves of the H6-III inverter are illustrated in Fig. 3.35 [5, 10].

3.8.4 H6-IV topology

The H6-IV inverter topology, which includes six switches and two freewheeling diodes as shown in Fig. 3.36, was proposed by Cui et al. [25]. The S_1-S_4 switches are switched using hybrid SPWM in the following analyses. The S_1-S_2 switches are operated in fundamental frequency while the S_3-S_4 switches are triggered at the carrier frequency, as depicted in Fig. 3.37. In the positive half-cycle, S_1 is turned to the "ON" state and S_2, S_3, and S_6 are turned to the "OFF" state, while S_4 and S_5 are switched at the carrier frequency. In the negative half-cycle, S_3 and S_6 are switched at

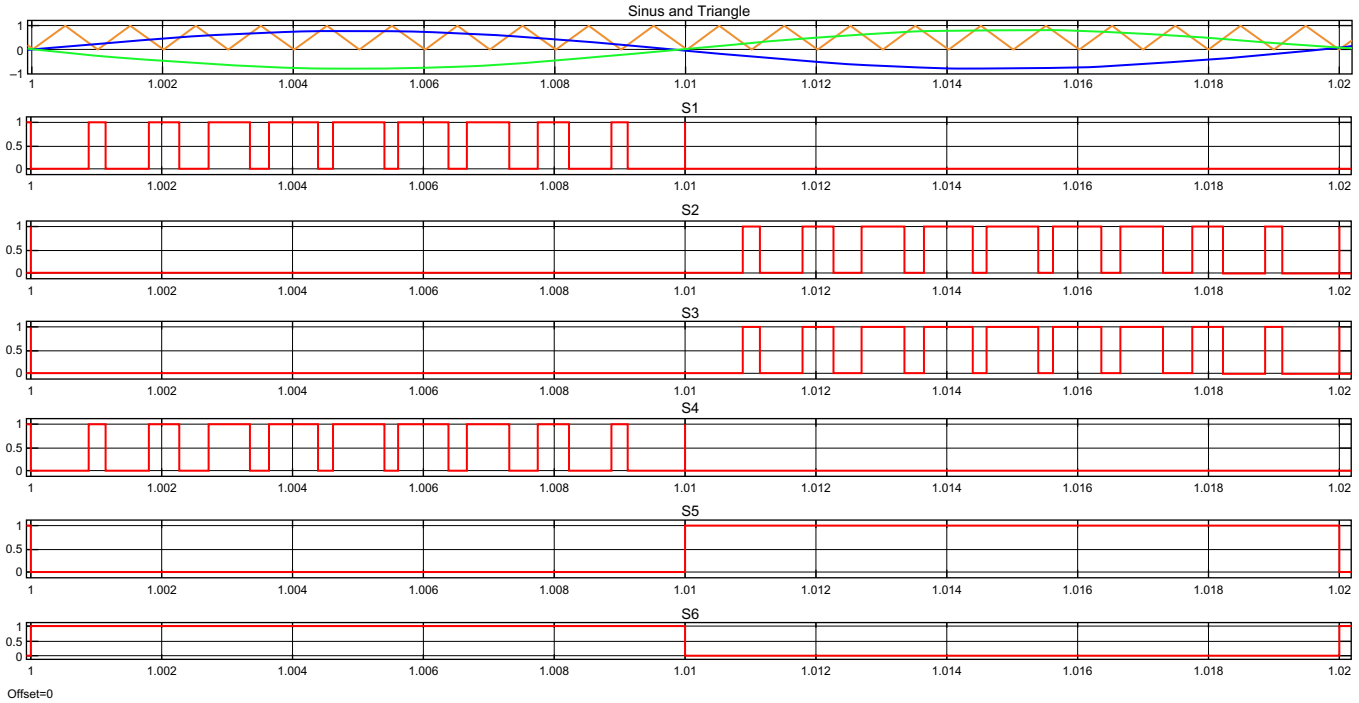

FIG. 3.30

Switching signals in H6-I inverter topology.

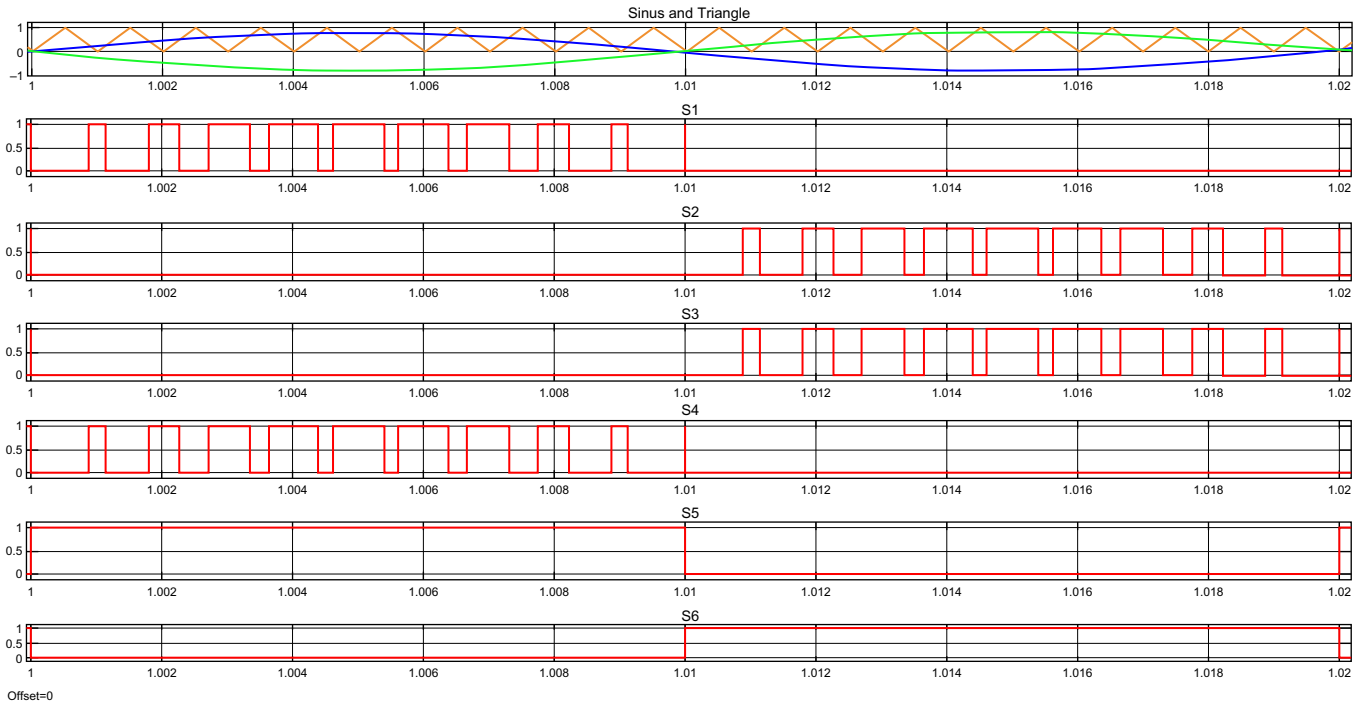

FIG. 3.31

Switching signals in H6-II inverter topology.

Table 3.9 Switching states of H6-I topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4-S_6	S_2-S_3-S_5	$+V_{DC}$
Freewheeling mode-I	S_6-D_1	S_1-S_2-S_3-S_4-S_5	0
Freewheeling mode-II	S_5-D_2	S_1-S_2-S_3-S_4-S_6	0
Negative half-cycle	S_2-S_3-S_5	S_1-S_4-S_6	$-V_{DC}$

Table 3.10 Switching states of H6-II topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4-S_5	S_2-S_3-S_6	$+V_{DC}$
Freewheeling mode-I	S_5-D_1	S_1-S_2-S_3-S_4-S_6	0
Freewheeling mode-II	S_6-D_2	S_1-S_2-S_3-S_4-S_5	0
Negative half-cycle	S_2-S_3-S_6	S_1-S_4-S_5	$-V_{DC}$

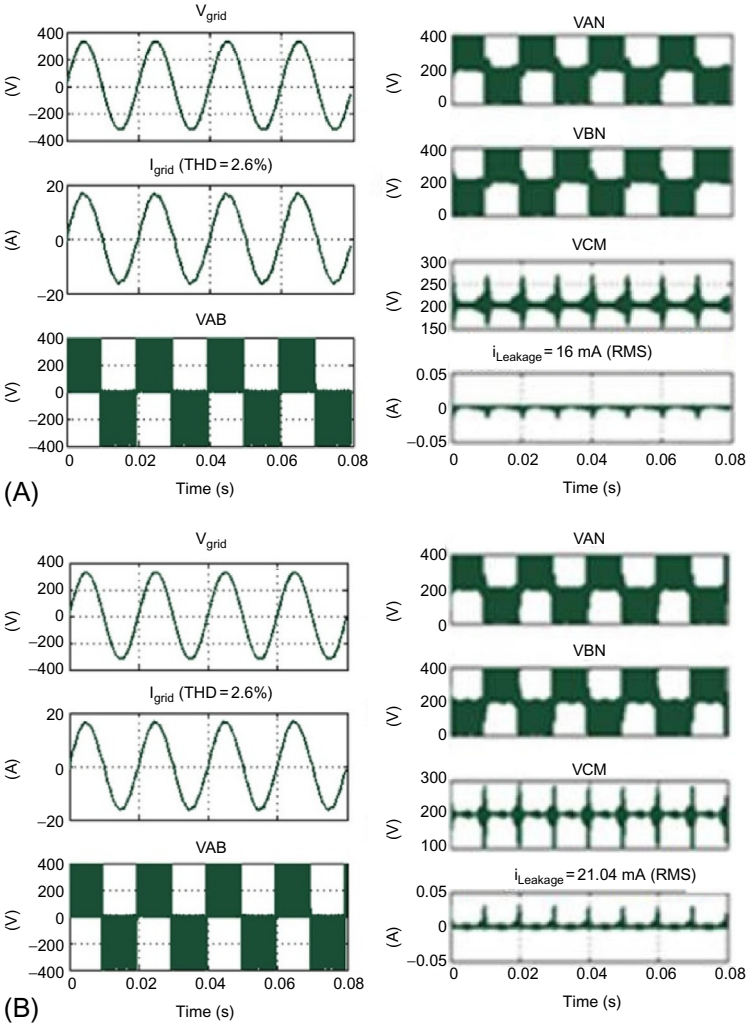

FIG. 3.32

Characteristic output waves of inverter: (A) H6-I topologies, (B) H6-II inverter topologies [10].

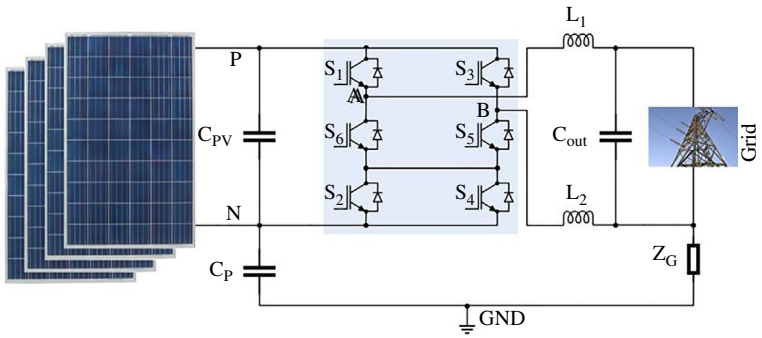

FIG. 3.33

H6-III inverter topology.

the carrier frequency, while S_2 is at the "ON" state and S_1, S_4, and S_5 are at the "OFF" state. The current path of freewheeling mode-I follows S_1-D_1 and the current path of freewheeling mode-II follows the S_2-D_2 path. The switching states of the modes are depicted in Table 3.12 [10, 25].

The simulation results of the H6-IV inverter are illustrated in Fig. 3.38, which has been represented in [10]. The CMV is not constant and oscillates during freewheeling periods; therefore the leakage current increases to 11 mA and it is not reduced completely [10].

3.8.5 Passive clamped H6 topology

The passive clamped H6 topology was proposed by Gonzalez et al. [26] as shown in Fig. 3.39. There are six switches (S_1-S_6) and two diodes (D_1 and D_2) in this structure. The diodes are connected to the middle point of voltage-divider capacitors. The connections of switching devices are configured similarly to the H6 inverter, but the switching states are different from the H6 inverter. The diodes D_1 and D_2 clamp the DC bus voltage to the V/2 level in the freewheeling mode. The switching states are illustrated in Fig. 3.40, where S5 and S6 switches are used to disconnect the grid from the PV in freewheeling mode [10, 26].

The operation of the topology in the power transfer stage and freewheeling modes is illustrated in Table 3.13. During the positive half-cycle, S_1 and S_4 are switched to the "ON" state, and S_5 and S6 are switched at the carrier frequency. Also, S_2 and S_3 are turned to the "ON" state, and S_5 and S_6 are switched at the carrier frequency in the negative half-cycle. The freewheeling modes of the passive clamped H6 topology are achieved at V/2 levels with clamping diodes and capacitors [10, 26].

The characteristic output waveforms of the passive clamped H6 inverter are depicted in Fig. 3.41 by simulation study of [10]. The inverter characteristics are improved due to clamping of CMV to the V/2 level, where the CMV is constant, unlike the H6 topology, and leakage current is very low, at 5.1 mA [10].

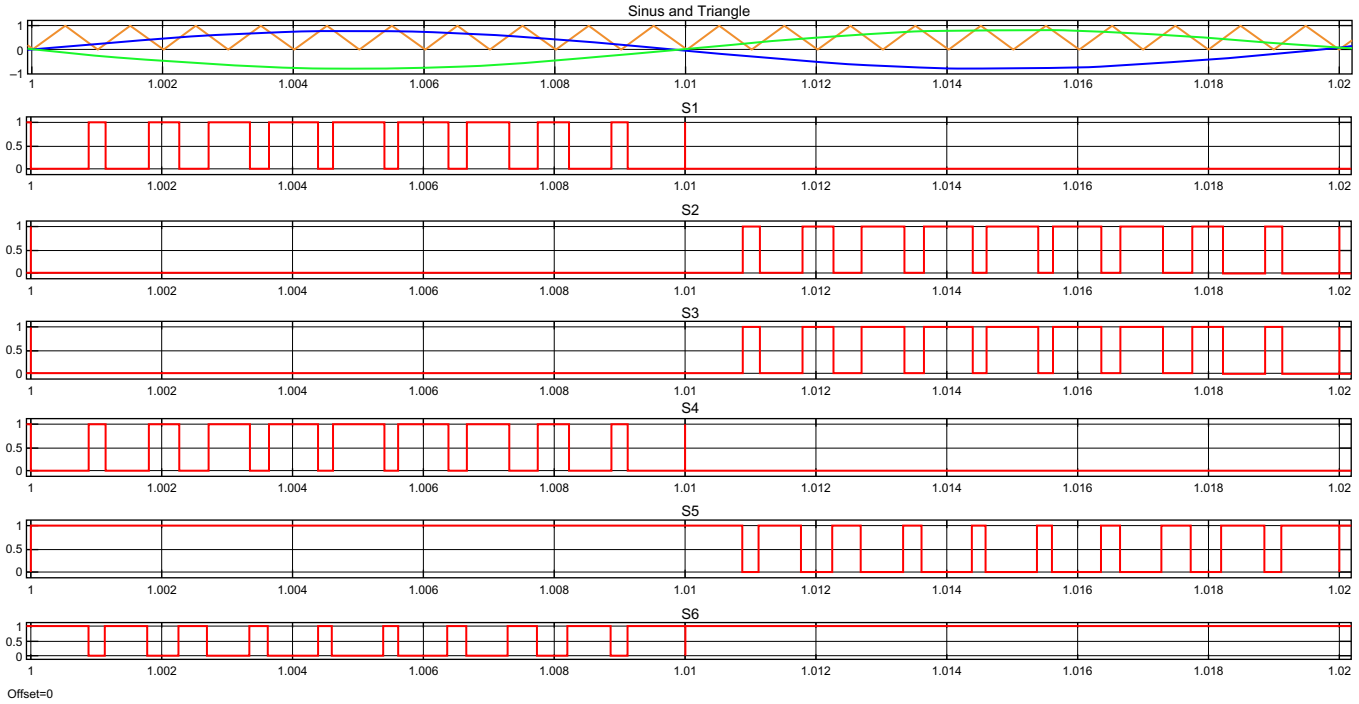

FIG. 3.34

Switching signals in H6-III inverter topology.

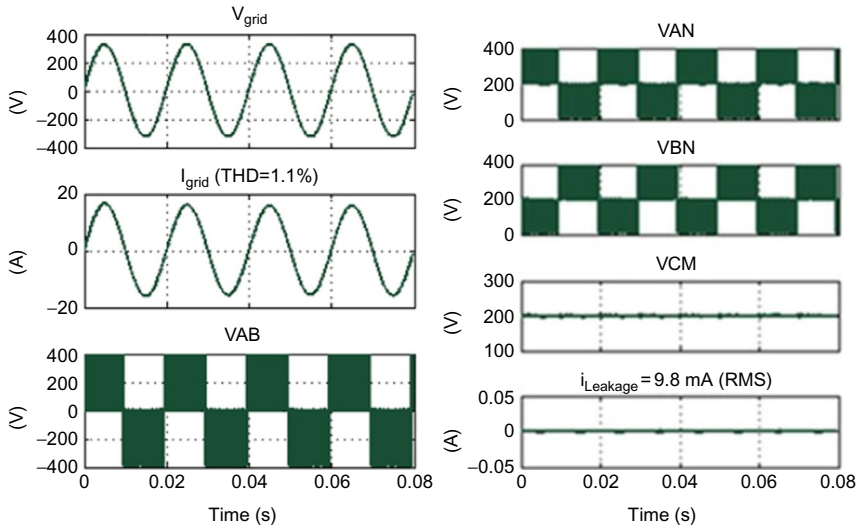

FIG. 3.35

Characteristic output waves of H6-III inverter [10].

Table 3.11 Switching states of H6-III topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4-S_5	S_2-S_3-S_6	$+V_{DC}$
Freewheeling mode-I	S_5-S_6(antiparallel diode)	S_1-S_2- S_3-S_4	0
Freewheeling mode-II	S_6-S_5(antiparallel diode)	S_1-S_2- S_3-S_4	0
Negative half-cycle	S_2-S_3-S_5	S_1-S_4-S_6	$-V_{DC}$

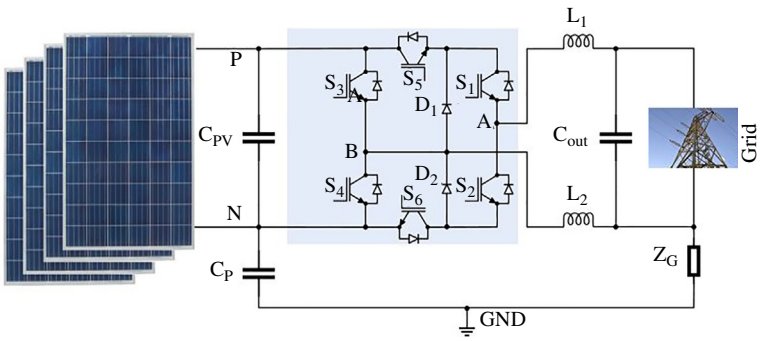

FIG. 3.36

H6-IV inverter topology.

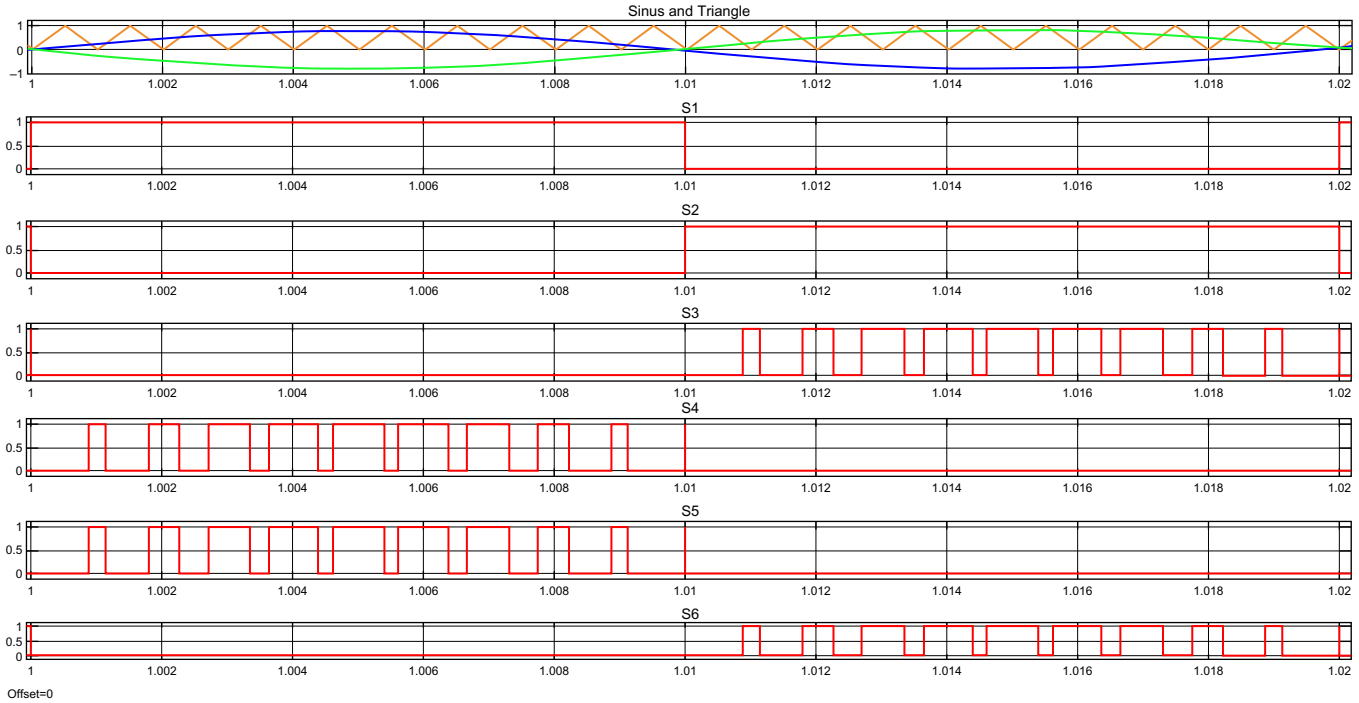

FIG. 3.37

Switching signals in H6-IV inverter topology.

Table 3.12 Switching states of H6-IV topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4-S_5	S_2-S_3-S_6	$+V_{DC}$
Freewheeling mode-I	S_1-D_1	S_2-S_3-S_4-S_5-S_6	0
Freewheeling mode-II	S_2-D_2	S_2-S_3-S_4-S_5-S_6	0
Negative half-cycle	S_2-S_3-S_6	S_1-S_4-S_5	$-V_{DC}$

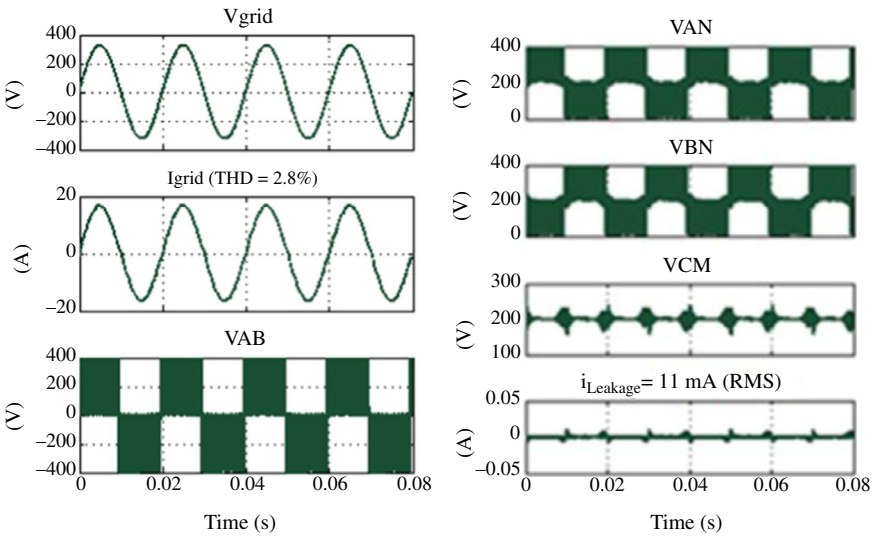

FIG. 3.38

Characteristic output waves of H6-IV inverter [10].

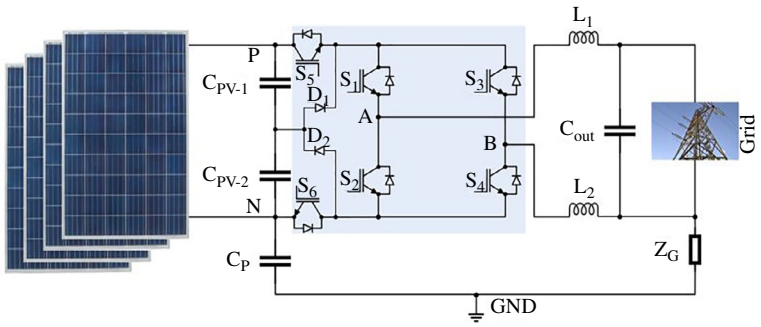

FIG. 3.39

Passive clamped H6 inverter topology.

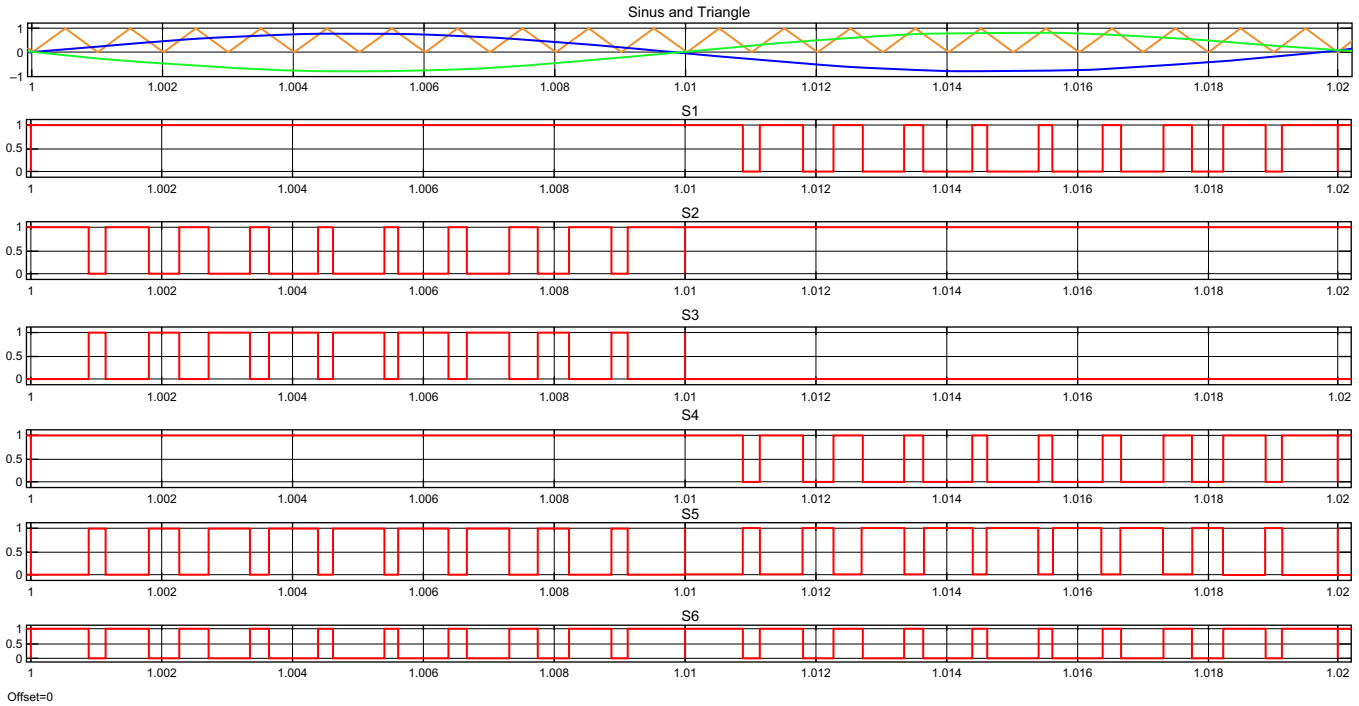

FIG. 3.40

Switching signals in passive clamped H6 inverter topology.

Table 3.13 Switching states of passive clamped H6 topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-wave	S_1-S_4-S_5-S_6	S_2-S_3	$+V_{DC}$
Freewheeling mode-I	S_1-S_3(antiparallel diode)	S_2-S_4-S_5-S_6	0
Freewheeling mode-II	S_3-S_1(antiparallel diode)	S_2-S_4-S_5-S_6	0
Negative half-wave	S_2-S_3-S_5-S_6	S_1-S_4-S_6	$-V_{DC}$

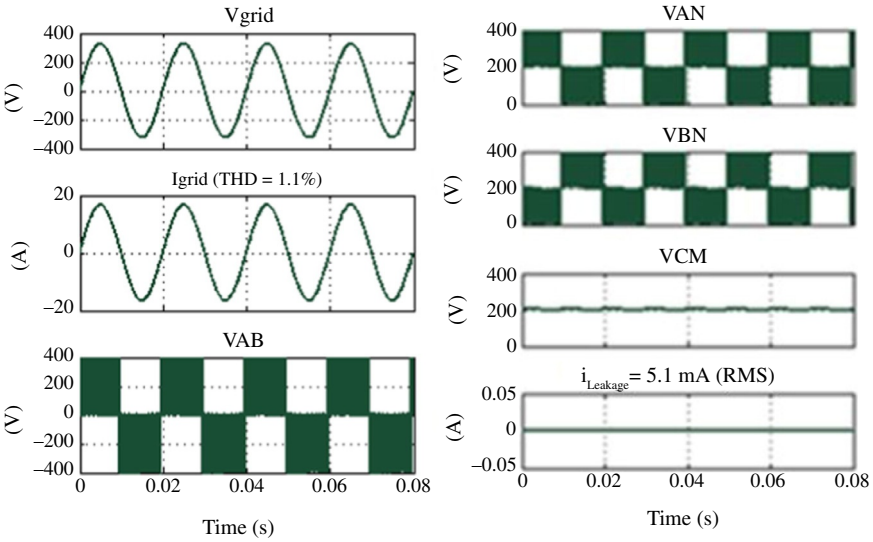

FIG. 3.41

Characteristic output waves of passive clamped H6 inverter [10].

3.8.6 HB-ZVR topology

The H-bridge zero voltage rectifier (HB-ZVR) topology was proposed by Kerekes et al. [27]. This topology provides constant CMV in freewheeling mode. The HB-ZVR topology is based on the H4 topology with an active switch (S_5), a full bridge rectifier (D_1-D_4), clamping capacitors ($C_{PV\text{-}1}$ and $C_{PV\text{-}2}$) and a clamping diode (D_5) are included in the topology, as depicted in Fig. 3.42. This inverter topology forms an AC bypass with a rectifier bridge in freewheeling mode, similarly to the HERIC inverter [10, 27].

Operating states of the switching signal are shown in Fig. 3.43, and the current path of the HB-ZVR topology is depicted in Table 3.14. The inverter operates like an H4 topology in positive and negative half-cycles. The S_5 and rectifier bridge diodes operate in freewheeling mode. The S_5 switch functions complementarily for S_1 and

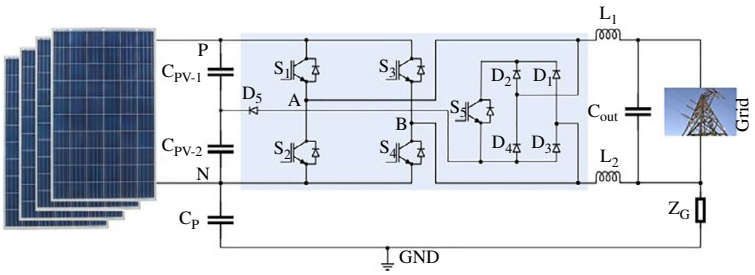

FIG. 3.42

HB-ZVR inverter topology.

S_4 in the positive half-cycle and S_2 and S_3 in the negative half-cycle. However, there must be dead time between H-bridge switches (S_1-S_4 or S_2-S_3) and the S_5 switch to protect the inverter from short circuits caused by clamping capacitors that are linear without fluctuation [10, 27].

Characteristic output waveforms of the HB-ZVR inverter are depicted in Fig. 3.44. HB-ZVR provides decreased leakage current compared to the HERIC inverter, which has an AC bypass structure. The leakage current of the HB-ZVR is 12.7 mA, while the THD ratio is the same as that of the HERIC inverter [10].

3.8.7 HBZVR-D topology

The H-bridge zero voltage rectifier-diode type topology (HBZVR-D) was proposed by Freddy et al. [21]. This topology is similar to the HBZVR, including an additional clamping diode in the structure connected to the middle point of the clamping diodes, as given in Fig. 3.45. Rectifier diodes comprise the zero-voltage state in freewheeling mode. The switching states are given in Fig. 3.46, where S_1, S_2, S_3, and S_4 switches play an active role in positive and negative half-cycle, and the devices are switched at the carrier frequency. S_5 is at the "ON" state while H-bridge switches are turned "OFF" in freewheeling modes.

The operations of switching states are depicted in Table 3.15. This is an improved version of HBZVR. The voltages of the D_{10} and D_{11} diodes clamp CMV to the $V_{DC}/2$ value in freewheeling modes. As a result, the leakage current is reduced to 5.4 mA and the THD ratio is detected as 1.2%, as illustrated in Fig. 3.47 [10, 21].

3.8.8 Active clamped HERIC topology

The active clamped HERIC configuration is an improved topology of the HERIC inverter from Li et al. [28]. This topology includes seven switches, where six (S_1, S_2, S_3, S_4 and S_A, S_B) are the same as in the HERIC inverter, as depicted in Fig. 3.48. An additional switch (S_C) is a clamping AC bypass switch proposed for clamping capacitors in freewheeling mode [10, 28].

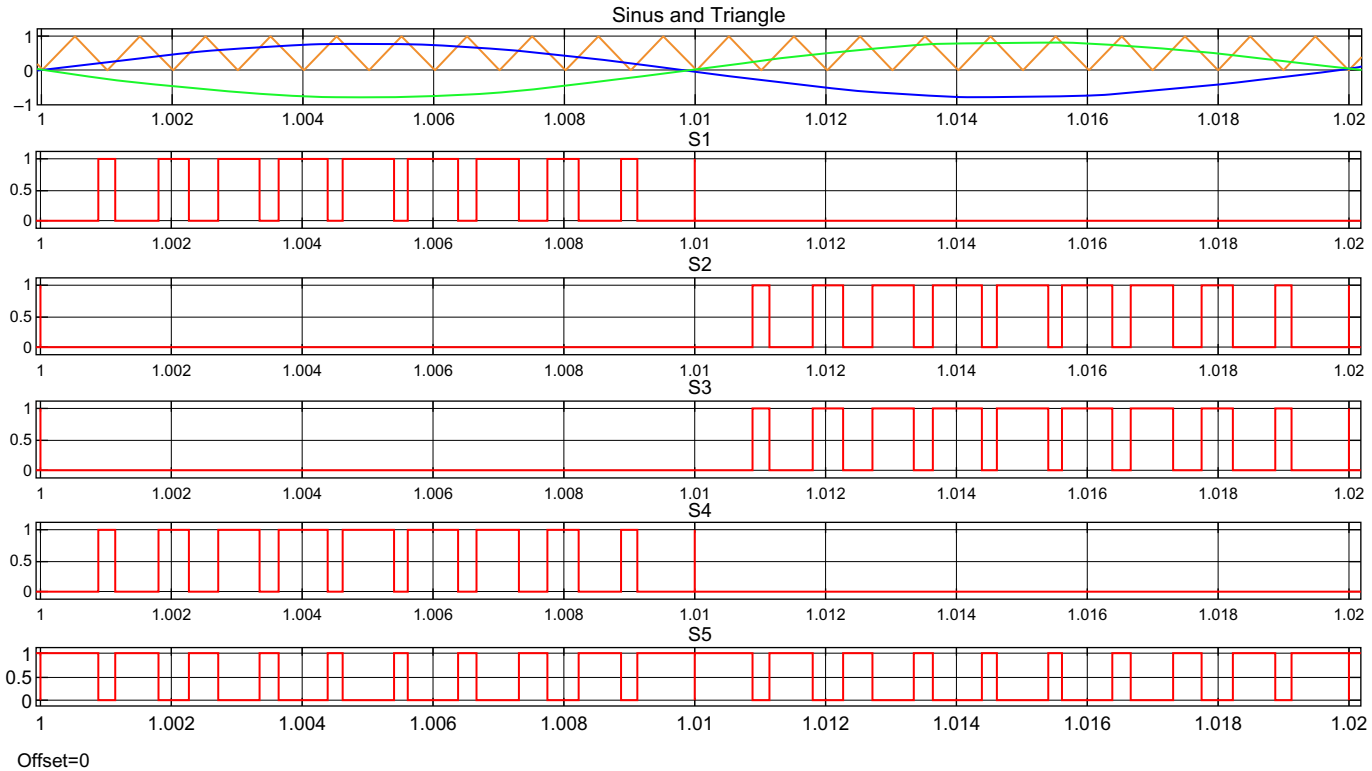

FIG. 3.43

Switching signals in HB-ZVR inverter topology.

Table 3.14 Switching states of HB-ZVR topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4	S_2-S_3	$+V_{DC}$
Freewheeling mode-I	S_5 and (D_1-D_3)	S_1-S_2-S_3-S_4	0
Freewheeling mode-II	S_5 and (D_2-D_4)	S_1-S_2-S_3-S_4	0
Negative half-cycle	S_2-S_3	S_1-S_4	$-V_{DC}$

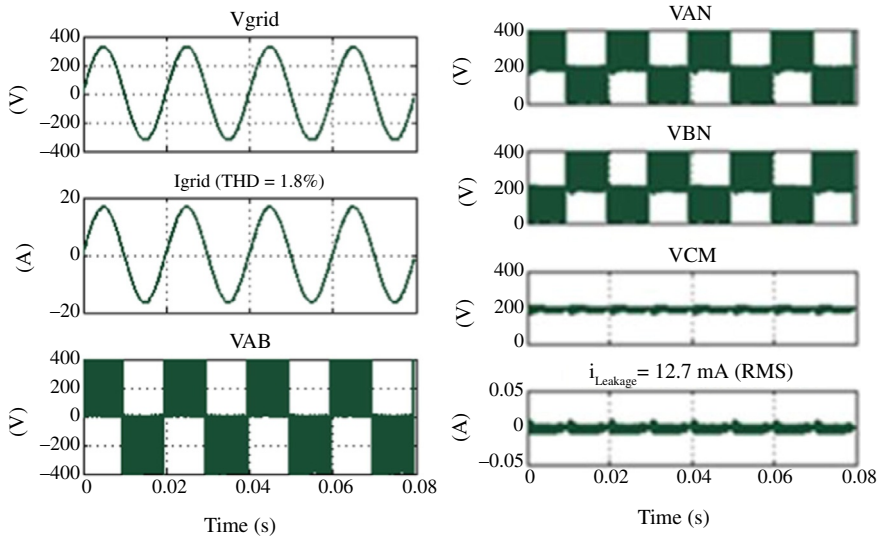

FIG. 3.44

Characteristic output waveforms of HB-ZVR inverter [10].

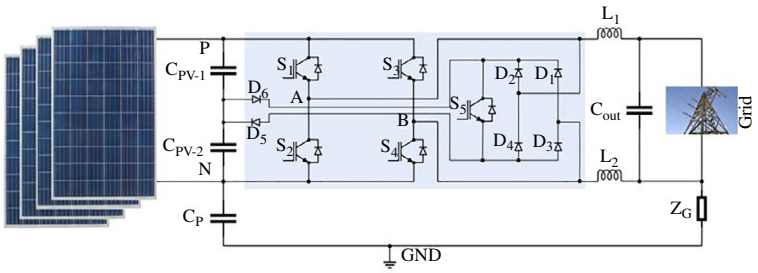

FIG. 3.45

HBZVR-D inverter topology.

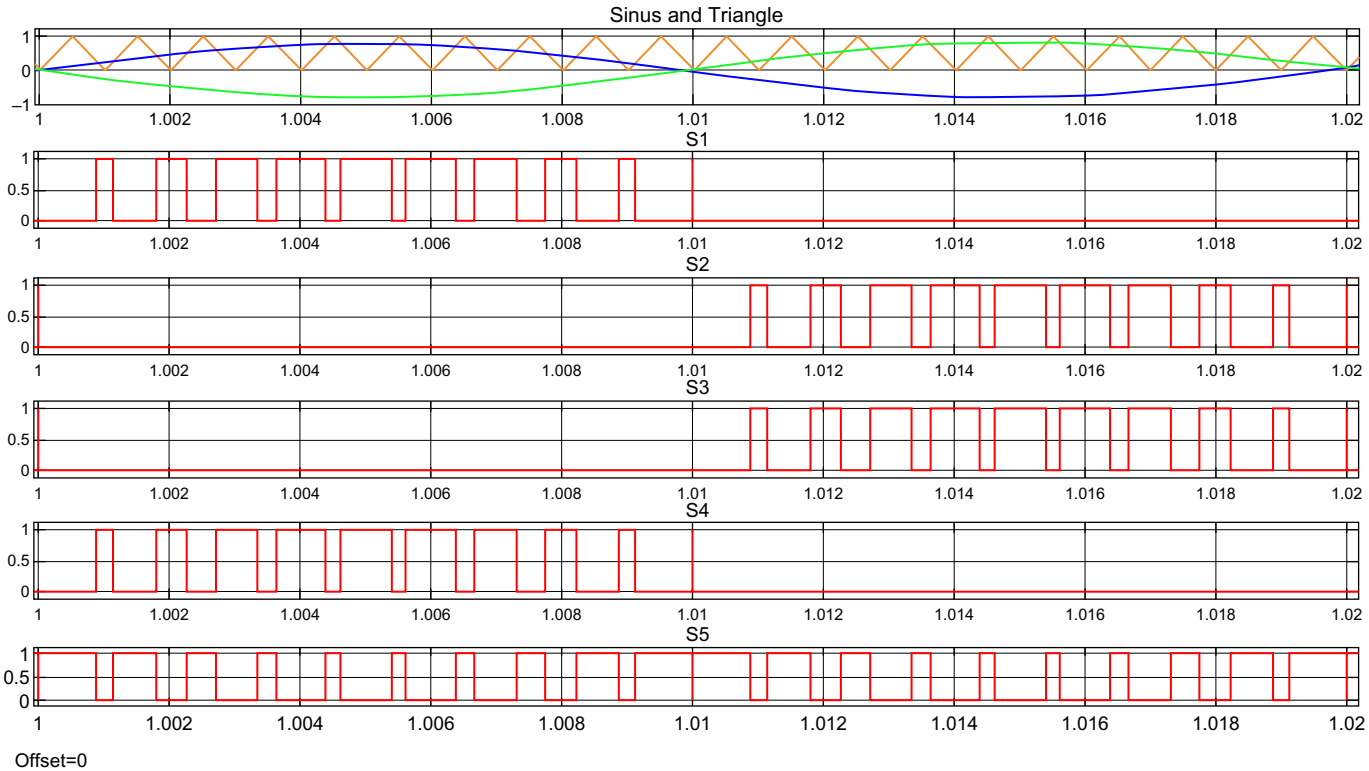

FIG. 3.46

Switching signals in HBZVR-D inverter topology.

Table 3.15 Switching states of HBZVR-D topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4	S_2-S_3	$+V_{DC}$
Freewheeling mode-I	S_5 and (D_1-D_3)	S_1-S_2-S_3-S_4	0
Freewheeling mode-II	S_5 and (D_2-D_4)	S_1-S_2-S_3-S_4	0
Negative half-cycle	S_2-S_3	S_1-S_4	$-V_{DC}$

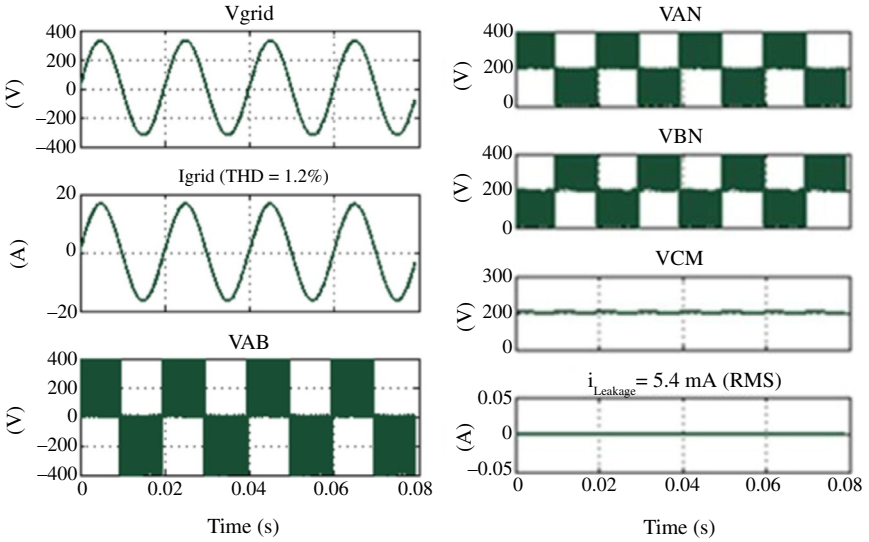

FIG. 3.47

Characteristic output waveforms of HBZVR-D inverter [10].

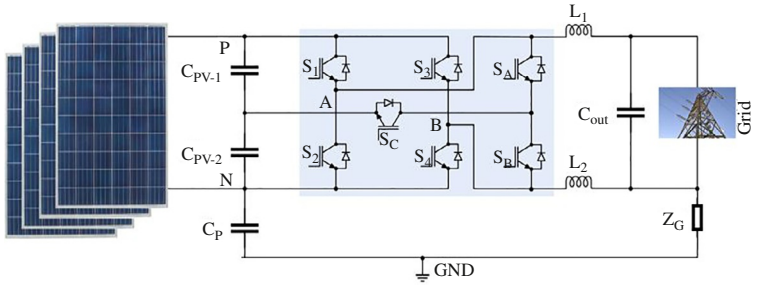

FIG. 3.48

Active clamped HERIC inverter topology.

The operating principle of the switches is illustrated in Fig. 3.49. The H-bridge switches are operated at carrier frequency as well as using the unipolar SPWM strategy. S_A and S_B are switched depending on the polarity of the output. In the positive half-cycle, S_A is "ON" and S_B is switched at carrier frequency as complementary of S_1 and S_4, while S_B is "ON" and S_A is switched at carrier frequency as complementary of S_2 and S_3 at the negative half-cycle. The freewheeling mode is given in Table 3.16. The switch S_C is not included in the freewheeling mode, but it is operated for clamping the output of the inverter. Characteristic output waveforms of active clamped HERIC inverter are shown in Fig. 3.50 [10].

3.9 Remarks and conclusion

The integration of multilevel inverters to distributed generation systems is implemented by using isolated or nonisolated topologies according to their galvanic isolation. Leakage current, efficiency, EMI, THD, and safety problems are commonly met with in nonisolated systems due to the absence of galvanic isolation. However, this issue can be tackled by using capacitive isolation.

Fundamental safety problems are caused by leakage current, which is produced by the fluctuation of CMV and parasitic capacitance between PV neutral and grid neutral, as handled in this chapter. Different SPWM strategies including bipolar, unipolar, and hybrid are used for switching classical H4 inverters. There are some advantages and disadvantages of these techniques. The output voltage of bipolar SPWM oscillates between $+V_{DC}$ and $-V_{DC}$ and these variations increase the dV/dt and THD ratios. However, no freewheeling period exists in the bipolar SPWM method and this provides minimum fluctuation of CMV and minimum leakage current. The unipolar and hybrid SPWM strategies oscillate between $+V_{DC}$, 0, and $-V_{DC}$.

Many new topologies are being proposed by researchers that are based on the H-bridge. The most common topologies are H5, H6, and HERIC. Also, there are recent H-bridge based topologies, such as oH5, H6-I, H6-II, H6-III, H6-IV, passive clamped H6, HB-ZVR, HBZVR-D and active clamped HERIC topologies. The purpose of these topologies is to reduce the leakage current and THD ratio. They are based on use of different numbers of switching components. Furthermore, some of them use extra diodes or capacitors in their structure. A comparison of topologies related to the component numbers is given in Table 3.17, where different component numbers are used in topologies due to the structure. The number of the switch is an important value in the structure, since if the number of switches is increased, the driven circuit number and cost of the system increases. Also, switches in the active current path (positive or negative half-cycle) are given in Table 3.17. When the number of active switch decreases, switching power loss of the system decreases. Topologies can be classified into two categories: DC bypass and AC bypass topologies. The important parameters of a nonisolated grid-tie PV inverter are leakage current and THD value. Leakage current values in different topologies are referred to the

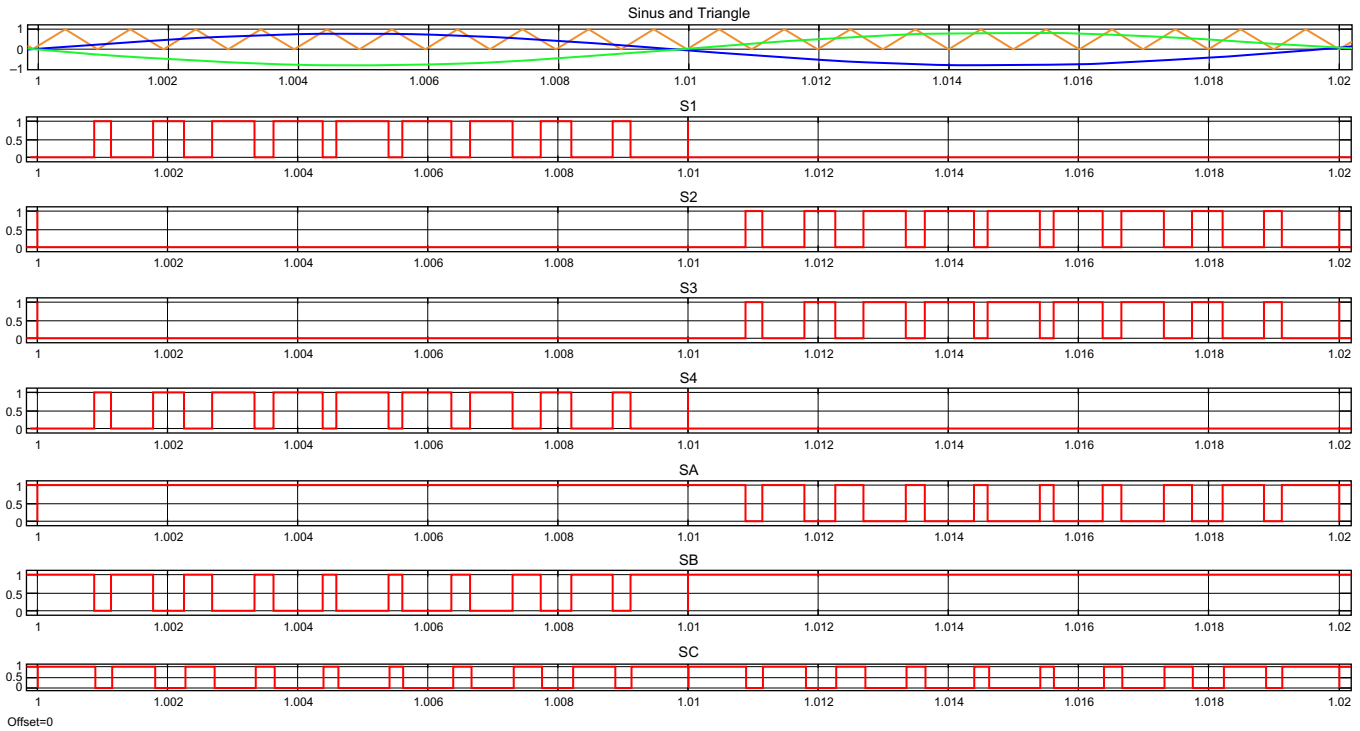

FIG. 3.49

Switching signals in active clamped HERIC inverter topology.

Table 3.16 Switching states of active clamped HERIC topology.

Switching state	"ON" state switches	"OFF" state switches	V_{out}
Positive half-cycle	S_1-S_4	S_2-S_3-S_5-S_6	$+V_{DC}$
Freewheeling mode-I	S_A-S_B(antiparallel diode)	S_1-S_2-S_3-S_4	0
Freewheeling mode-II	S_B-S_A(antiparallel diode)	S_1-S_2-S_3-S_4	0
Negative half-cycle	S_2-S_3	S_1-S_4-S_5-S_6	$-V_{DC}$

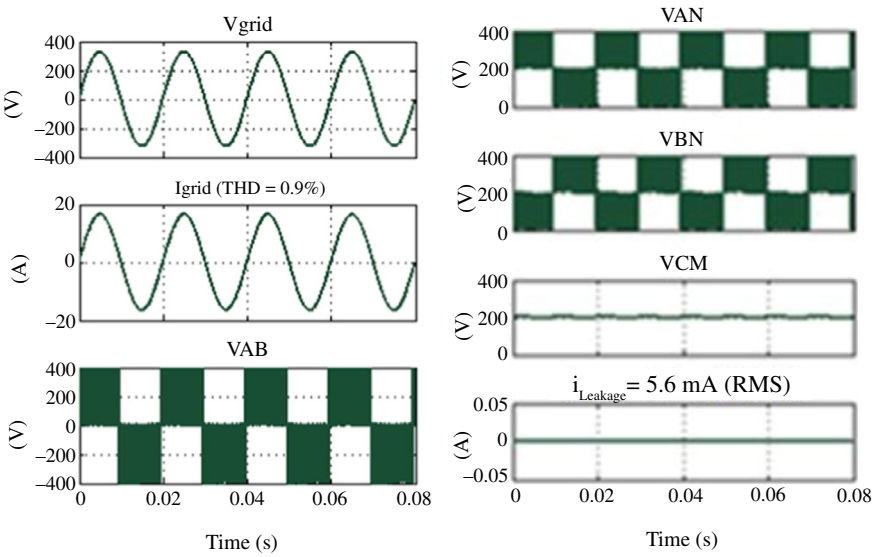

FIG. 3.50

Characteristic output waveforms of active clamped HERIC inverter [10].

simulations of [10], which are depicted in Fig. 3.51. The passive clamped H6 topology has the lowest leakage current values, but when comparing the total number of components and active switch in the current path with leakage current, the oH5 topology can be chosen due to its minimized device numbers and resultant efficiency. It is seen that the THD values of the topologies are close to each other and comply with the standards. The clamped CMV topologies provide reduced leakage current and THD value. The aim of these topologies is to produce constant CMV and minimum leakage current and THD values. Also, disconnection of PV panels from the grid neutral in freewheeling modes is allowed by these topologies.

Table 3.17 Comparison of nonisolated grid-tied H-bridge based topologies.

Inverter Topology	Total number of switches	Switches in the active current path	Switches in f path	Bypass mode	Leakage current	Input capacitor	THD (%)
H4 topology (Unipolar SPWM)	4S	2S	1 S	—	1.8 A	1	2.8
H4 topology (Hybrid SPWM)	4S	2S	1S + 1D	—	3.9 A	1	3
H4 topology (Bipolar SPWM)	4S	2S	1S + 1D	—	15.4 mA	1	1.8
H5 topology	5S	3S	1S + 1D	DC	23.4 mA	1	1
H6 topology	6S	4S	1S + 1D	DC	16.09 mA	1	1.1
HERIC topology	6S	2S	1S + 1D	AC	23.5 mA	1	1.7
H6-I topology	6S + 2D	3S	1S + 1D	DC	16 mA	1	2.6
H6-II topology	6 S + 2D	3S	1S + 1D	DC	21.4 mA	1	2.3
H6-III topology	6S	3S	1S + 1D	DC	9.8 mA	1	1.1
H6-IV topology	6S + 2D	3S	1S + 1D	DC	11 mA	1	2.8
Optimized H5 topology	6S	3S	1S + 1D	DC	5.8 mA	2	1
Passive clamped H6 topology	6S + 2D	4S	1S + 1D	DC	5.1 mA	2	1.1
HB-ZVR topology	5S + 5D	2S	1S + 2D	AC	12.7 mA	2	1.8
ZVBR-D topology	5S + 6D	2S	1S + 2D	AC	5.4 mA	2	1.2
Active clamped HERIC topology	7S	2S	1S + 1D	AC	5.6 mA	2	0.9

S = Switch, D = Diode, f = Freewheeling mode.

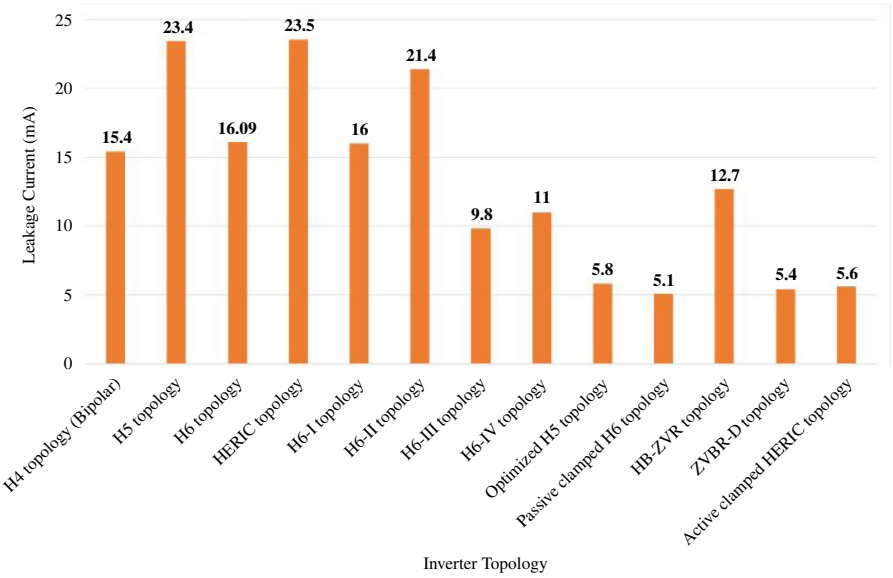

FIG. 3.51

Leakage current values in different topologies.

References

[1] E. Kabalcı, Review on novel single-phase grid-connected solar inverters: circuits and control methods, Solar Energy. 198 (2020) 247–274, https://doi.org/10.1016/j.solener.2020.01.063.

[2] M. Islam, S. Mekhilef, M. Hasan, Single phase transformerless inverter topologies for grid-tied photovoltaic system: a review, Renew. Sustain. Energy Rev. 45 (2015) 69–86, https://doi.org/10.1016/j.rser.2015.01.009.

[3] S. Chaudhary, S.N. Singh, in: Single phase grid interactive solar photovoltaic inverters: a review, 2018 National Power Engineering Conference, NPEC, 2018, 2018, pp. 1–6, https://doi.org/10.1109/NPEC.2018.8476767.

[4] A.A. Estévez-Bén, A. Alvarez-Diazcomas, G. Macias-Bobadilla, J. Rodríguez-Reséndiz, Leakage current reduction in single-phase grid-connected inverters—a review, Appl. Sci. 10 (2020) 2384. https://doi.org/10.3390/app10072384.

[5] M. Islam, S. Mekhilef, H6-type transformerless single-phase inverter for grid-tied photovoltaic system, IET Power Electron. 8 (2015) 636–644, https://doi.org/10.1049/iet-pel.2014.0251.

[6] N.M.J.S. Kirthiga, Highly reliable inverter topology with a novel soft computing technique to eliminate leakage current in grid-connected transformerless photovoltaic systems, Comput. Electr. Eng. 68 (2018) 192–203. https://doi.org/10.1016/j.compeleceng.2018.03.022.

[7] R.H. Baker, L.H. Bannister, Electric power converter, U.S. Patent No. 3,867,643. 18 Feb, 1975.

[8] M. Vijeh, M. Rezanejad, E. Samadaei, K. Bertilsson, A general review of multilevel inverters based on Main submodules: structural point of view, IEEE Trans. Power Electron. 34 (2019) 9479–9502, https://doi.org/10.1109/TPEL.2018.2890649.
[9] P.S. Gotekar, S.P. Muley, D.P. Kothari, B.S. Umre, Comparison of full bridge bipolar, H5, H6 and HERIC inverter for single phase photovoltaic systems—a review, 12th IEEE International Conference Electronics, Energy, Environment, Communication, Computer, Control: (E3-C3), INDICON 2015. (2016) 1–6. doi:https://doi.org/10.1109/INDICON.2015.7443837.
[10] Z. Ahmad, S.N. Singh, Comparative analysis of single phase transformerless inverter topologies for grid connected PV system, Sol. Energy 149 (2017) 245–271, https://doi.org/10.1016/j.solener.2017.03.080.
[11] H. Albalawi, S.A. Zaid, An H5 transformerless inverter for grid connected PV systems with improved utilization factor and a simple maximum power point algorithm, Energies 11 (2018) 1–17, https://doi.org/10.3390/en11112912.
[12] K. Chen, Z. Huang, L. Hang, X. Xie, Q. Han, Q. Lu, Y. Gan, G. Yang, P. Shen, Cascaded iH6 multilevel inverter with leakage current reduction for transformerless grid-connected photovoltaic system, in: Proceedings of the International Conference on Power Electronics and Drive Systems, 2017, pp. 613–617, https://doi.org/10.1109/PEDS.2017.8289270. Decem (2018).
[13] Z. Özkan, Leakage Current and Energy Efficiency Analyses of Single Phase Grid Connected Multi-kVA Transformerless Photovoltaic Inverters, Middle East Technical University, 2012.
[14] T. Salmi, M. Bouzguenda, A. Gastli, A. Masmoudi, A novel transformerless inverter topology without zero-crossing distortion, International Journal of Renewable Energy Research 2 (2012) 140–146, https://doi.org/10.20508/ijrer.03543.
[15] A. Namboodiri, H. Wani, Unipolar and bipolar PWM inverter, IJIRSRT - International Journal for Innovative Research in Science & Technology 1 (2014) 7. http://www.ijirst.org/articles/IJIRSTV1I7111.pdf.
[16] Y.R. Kafle, G.E. Town, X. Guochun, S. Gautam, Performance comparison of single-phase transformerless PV inverter systems, in: Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2017, pp. 3589–3593, https://doi.org/10.1109/APEC.2017.7931213.
[17] G. Rizzoli, M. Mengoni, L. Zarri, A. Tani, G. Serra, D. Casadei, Comparison of single-phase H4, H5, H6 inverters for transformerless photovoltaic applications, in: IECON Proceedings (Industrial Electronics Conference), 2016, pp. 3038–3045, https://doi.org/10.1109/IECON.2016.7792984.
[18] K. Zeb, I. Khan, W. Uddin, M.A. Khan, P. Sathishkumar, T.D.C. Busarello, I. Ahmad, H. J. Kim, A review on recent advances and future trends of transformerless inverter structures for single-phase grid-connected photovoltaic systems, Energies 11 (2018) 1–33, https://doi.org/10.3390/en11081968.
[19] M.I. Alzoubi, A.M.T. Oo, S. Azad, Simulation and evaluation of HERIC and H5 transformerless inverter topologies, in: *Proceedings of the 6th IASTED Asian Conference on Power and Energy Systems*, AsiaPES, 2013, 2013, pp. 212–219, https://doi.org/10.2316/P.2013.800-101.
[20] A.J. Babqi, Z. Yi, D. Shi, X. Zhao, Model predictive control of H5 inverter for transformerless PV systems with maximum power point tracking and leakage current reduction, in: Proceedings: IECON 2018—44th Annual Conference of the IEEE Industrial Electronics Society, 2018, pp. 1860–1865, https://doi.org/10.1109/IECON.2018.8591386.

[21] T.K.S. Freddy, N.A. Rahim, W.P. Hew, H.S. Che, Comparison and analysis of single-phase transformerless grid-connected PV inverters, IEEE Trans. Power Electron. 29 (2014) 5358–5369, https://doi.org/10.1109/TPEL.2013.2294953.

[22] H. Xiao, S. Xie, Y. Chen, R. Huang, An optimized transformerless photovoltaic grid-connected inverter, IEEE Trans. Ind. Electron. 58 (2011) 1887–1895, https://doi.org/10.1109/TIE.2010.2054056.

[23] W. Yu, J.S. Lai, H. Qian, C. Hutchens, High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated AC-module applications, IEEE Trans. Power Electron. 26 (2011) 1253–1260, https://doi.org/10.1109/TPEL.2010.2071402.

[24] B. Ji, J. Wang, J. Zhao, High-efficiency single-phase transformerless PV H6 inverter with hybrid modulation method, IEEE Trans. Ind. Electron. 60 (2013) 2104–2115, https://doi.org/10.1109/TIE.2012.2225391.

[25] W. Cui, B. Yang, Y. Zhao, W. Li, X. He, A novel single-phase transformerless grid-connected inverter, in: IECON 2011—37th Annual Conference of the IEEE Industrial Electronics Society, 2011, pp. 1126–1130, https://doi.org/10.1109/IECON.2011.6119466.

[26] R. Gonzalez, J. Lopez, P. Sanchis, L. Marroyo, Transformerless inverter for single-phase photovoltaic systems, IEEE Trans. Power Electron. 22 (2007) 693–697, https://doi.org/10.1109/TPEL.2007.892120.

[27] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, E. Aldabas, A new high-efficiency single-phase transformerless PV inverter topology, IEEE Trans. Ind. Electron. 58 (2011) 184–191, https://doi.org/10.1109/TIE.2009.2024092.

[28] W. Li, Y. Gu, H. Luo, W. Cui, X. He, C. Xia, Topology review and derivation methodology of single-phase Transformerless photovoltaic inverters for leakage current suppression, IEEE Trans. Ind. Electron. 62 (2015) 4537–4551, https://doi.org/10.1109/TIE.2015.2399278.