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تعداد واحد: ۳ (نظری) پیشنیاز: -

همنياز: الكترونيك صنعتى

هدف: آشنایی با انواع روشهای کنترلی انواع مبدلهای ac-dc ،dc-ac ،dc-dc و ac-ac

- معرفی انواع شاخصهای لازم در طراحی مبدلهای الکترونیک قدرت
  - معرفی پارامترهای کارآیی برای انواع مبدلهای الکترونیک قدرت
- معرفی و نحوه پیادهسازی انواع روشهای مدولاسیون بردار فضایی، تکنیک مدولاسیون پهنای پالس (PWM)، شیفت فاز،
  باند هیسترزیس برای کنترل انواع مبدلهای الکترونیک قدرت در حالتهای متقارن و نامتقارن
  - معرفی و نحوه پیادهسازی انواع روشهای کنترلی شارژ متعادل برای اینورترهای چندسطحی



- [1] Gupta, Krishna Kumar, and Pallavee Bhatnagar. Multilevel inverters: conventional and emerging topologies and their control. Academic Press, 2017.
- [2] Gonzalez, S.A., Verne, S.A. and Valla, M.I., 2016. Multilevel converters for industrial applications. CRC Press.
- [3] Du, S., Dekka, A., Wu, B. and Zargari, N., 2017. Modular multilevel converters: analysis, control, and applications. John Wiley & Sons.

# فصل دوم [۱]

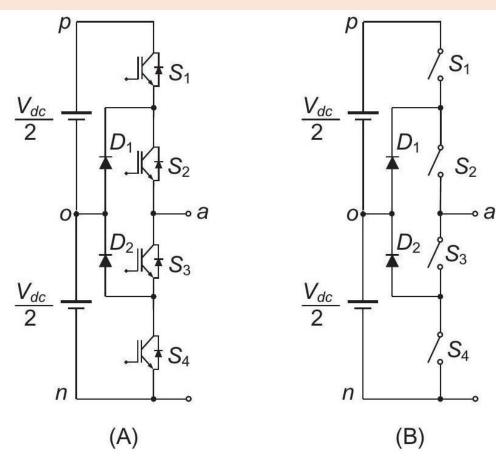
اساس مبدلهای چندسطحی

**\* 2.3.2 Diode-Clamped Structure and Modulation Strategies** 

#### 2.3.2 Diode-Clamped Structure and Modulation Strategies

NPC topology, which is also known as diode-clamped topology, started receiving attention when, in the 1980s, Nabae et al. demonstrated the implementation of an NPC inverter along with experimentation, using a pulse-width modulation scheme [3]. The topology, however, first appeared in a patent by Baker [4] in 1980. One leg of a three-level diode-clamped structure is shown in Fig. 2.14A.

√ فصل ۲ [۱]: اساس مبدلهای چندسطحی



**FIGURE 2.14** (A) One leg of a three-level diode-clamped inverter; (B) leg shown with "switches."

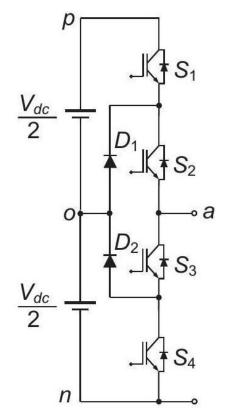
### روشهای نوین کنترل مبدلهای الکترونیک قدرت

√ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

As shown in Fig. 2.14A, the structure has a DC link voltage of  $V_{dc}$  which is generally halved using capacitors, but here it is shown with two DC

sources.

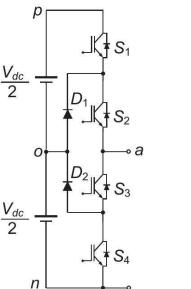


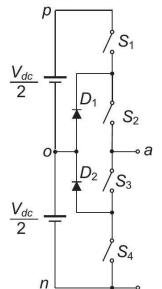
√ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

The leg consists of four bidirectional-conducting-unidirectional-blocking power switches. The clamping to the common point "o" is done with the help of two diodes,  $D_1$  and  $D_2$ . Positive and negative DC rails are shown with "p" and "n," respectively. In order to understand the workings, we replace the power switches with symbolic switches as shown in

Fig. 2.14B.





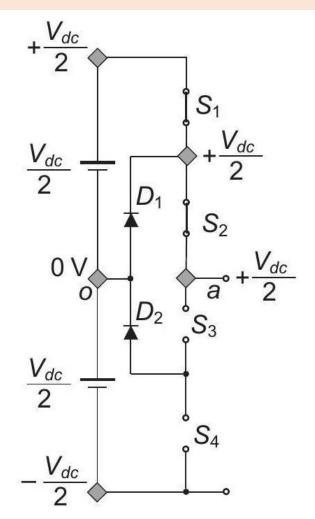
#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

There are three valid states for this structure, as depicted in Fig. 2.15. For analysis, point "o" is chosen as the reference node with a potential of 0 V. Accordingly, the potentials at p and n are  $+V_{dc}/2$  and  $-V_{dc}/2$ . The potential difference between Point "a" and "o" in the circuit is considered to be the load voltage,  $v_{ao}(t)$ . In State 1,  $S_1$  and  $S_2$  are simultaneously switched ON to obtain  $v_{ao}(t) = V_{dc}/2$ , as shown in Fig. 2.15A. It can be observed that the voltage stress across the devices in the OFF state is  $V_{dc}/2$  which is half the DC link voltage.

### روشهای نوین کنترل مبدلهای الکترونیک قدرت

### √ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**



#### State 1

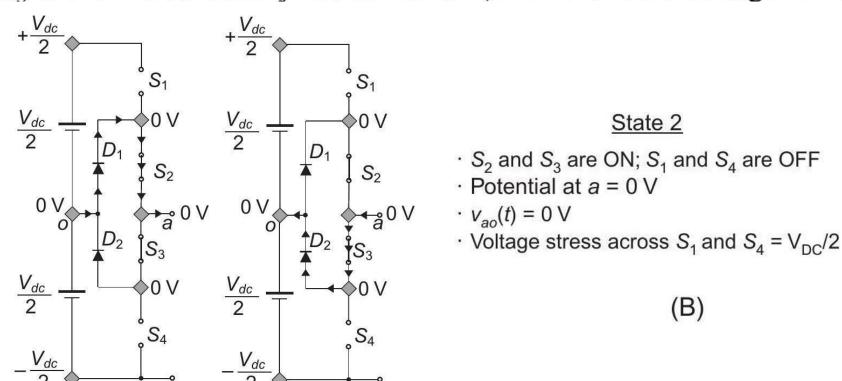
- $\cdot$   $S_1$  and  $S_2$  are ON;  $S_3$  and  $S_4$  are OFF
- · Potential at  $a = +V_{DC}/2$
- $\cdot v_{ao}(t) = V_{DC}/2$
- · Voltage stress across  $S_3$  and  $S_4 = V_{DC}/2$
- · Voltage stress across  $D_1$  and  $D_2 = V_{DC}/2$

(A)

### √ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

In State 2, two equivalent circuits are shown with directions of currents to emphasize the role of clamping diodes in the topology. When Switches  $S_2$  and  $S_3$  are simultaneously switched ON, then the load voltage is zero.



### √ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

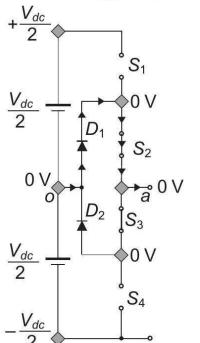
At this time, if the load current is positive, then the current completes its path through  $S_2$  and  $D_1$  as depicted in Fig. 2.15B. If the load current happens to be negative, then it completes its path through  $S_3$  and  $D_2$ , again depicted in Fig. 2.15B. Once again, the devices in the OFF

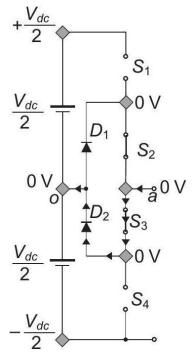
state block a voltage equal to  $V_{dc}/2$ .

#### State 2

- ·  $S_2$  and  $S_3$  are ON;  $S_1$  and  $S_4$  are OFF
- · Potential at a = 0 V
- $v_{ao}(t) = 0 \text{ V}$
- · Voltage stress across  $S_1$  and  $S_4 = V_{DC}/2$

(B)



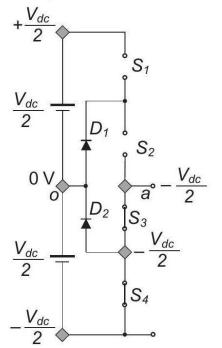


### √ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

In State 3, when Switches  $S_3$  and  $S_4$  are simultaneously turned ON, then the obtained load voltage is  $-V_{dc}/2$ , as shown in Fig. 2.15C. In this state also, the voltage stress across the OFF devices is  $V_{dc}/2$ . Hence, three levels are obtained using these three states:

 $\pm V_{dc}/2$  and 0.



#### State 3

- ·  $S_3$  and  $S_4$  are ON;  $S_1$  and  $S_2$  are OFF
- · Potential at  $a = -V_{DC}/2$
- $\cdot v_{ao}(t) = -V_{DC}/2$
- · Voltage stress across  $S_1$  and  $S_2 = V_{DC}/2$
- · Voltage stress across  $D_1$  and  $D_2 = V_{DC}/2$

(C)

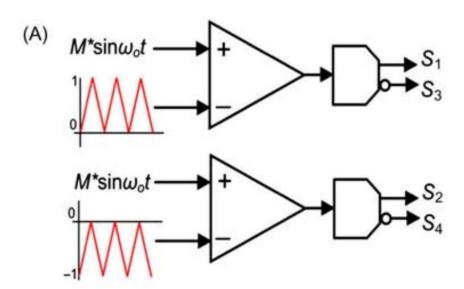
#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

In order to modulate this leg, the PWM scheme is as shown in Fig. 2.16A, along with the carrier and reference signals in Fig. 2.16B. A single reference is used, while two carrier signals are used. As opposed to the "phase-shifted" carrier signals used for the CHB topology, here the carrier signals are "level-shifted." That is to say, one carrier signal is above the zero reference and the other is below the zero reference.

√ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

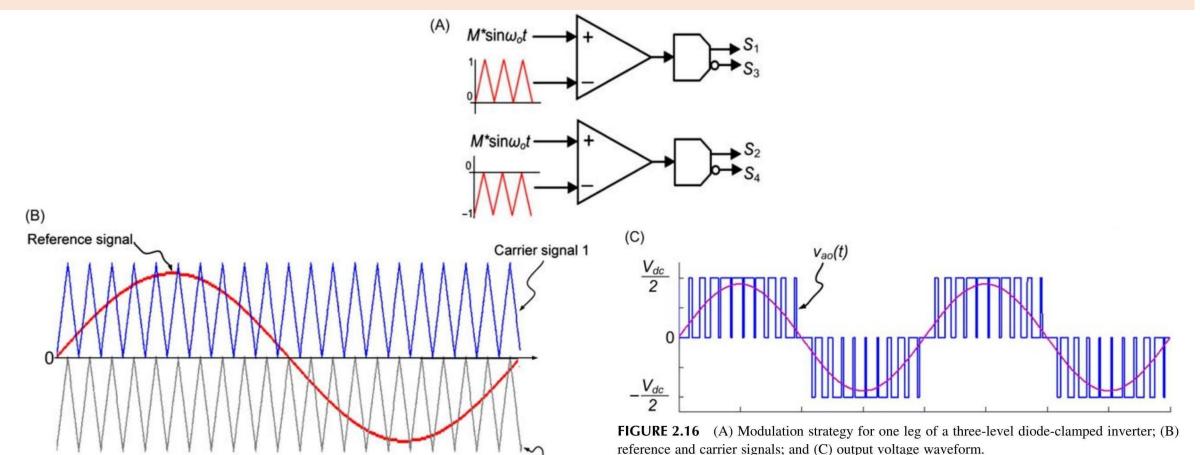
Whenever the reference signal is greater than the carrier signal 1, Switch  $S_1$  is turned ON, otherwise  $S_3$  is turned ON. Similarly, whenever the reference signal is greater than carrier signal 2, switch  $S_2$  is turned ON, otherwise Switch  $S_4$  is turned ON. When operated in this manner, the resulting load voltage  $v_{AO}(t)$  is as shown in Fig. 2.16C.



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# روشهای نوین کنترل مبدلهای الکترونیک قدرت ✓ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

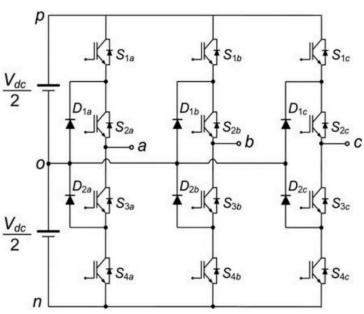


Carrier signal 2

#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

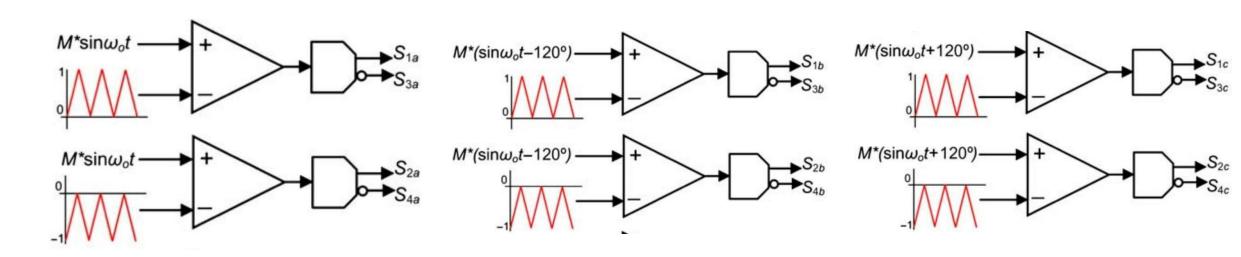
We have previously discussed that, for an MLI, generally, the voltage stress across the power switches is less than the operating voltage. This advantage can be seen here if three-phase voltage is obtained. A three-phase structure is obtained by "adding" to more three-level legs as shown in

Fig. 2.17.

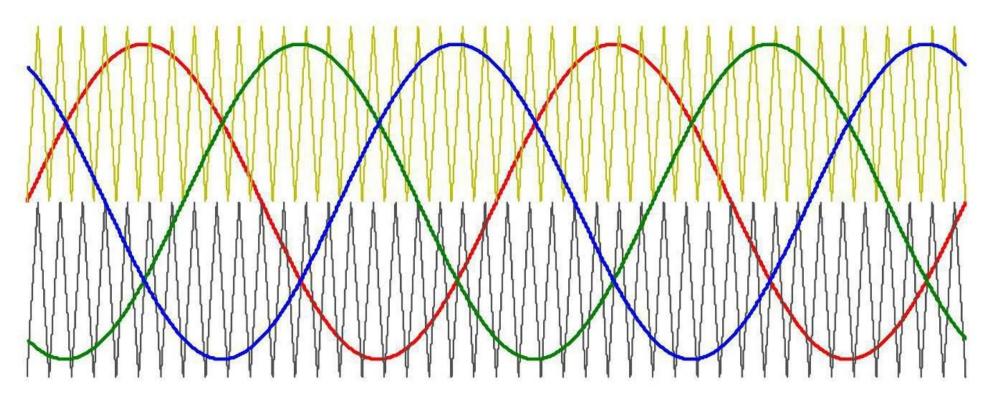


#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

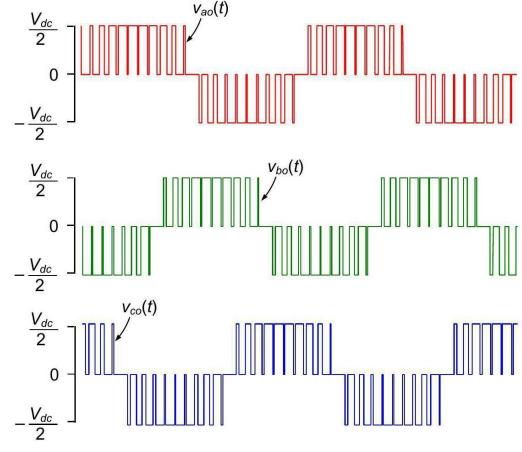
The three-phase structure can be modulated by modulating all three legs with level shifted carriers and sinusoidal references with a phase difference of  $120^{\circ}$ , as shown in Fig. 2.18. The corresponding carrier and reference signals are shown in Fig. 2.19. When modulated in this manner, the phase voltages have three levels, with  $V_{dc}/2$  as the peak value, and they are shifted from one another by an angle of 120 degrees, as shown in Fig. 2.20. The line voltages shown in Fig. 2.21 are all observed to consist of five levels. These are all phase-shifted from one another at an angle of 120 degrees and have a peak value of  $V_{dc}$ , which is twice the blocking voltage requirement.



**FIGURE 2.18** Modulation strategy for three-phase diode-clamped inverter with three-level legs.

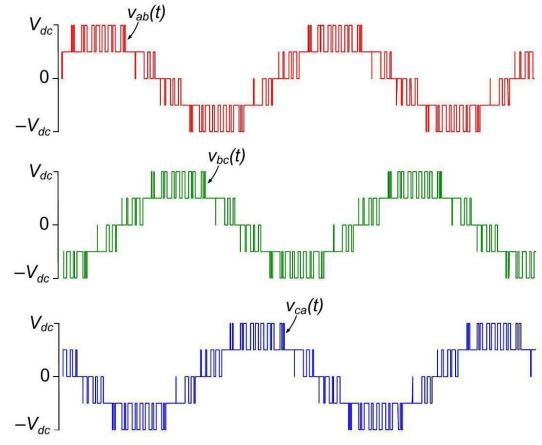


**FIGURE 2.19** Triangular carrier and sinusoidal reference signals for a three-phase diodeclamped inverter with three-level legs.



**FIGURE 2.20** Phase voltage waveforms for a three-phase diode-clamped inverter with three-level legs.

√ فصل ۲ [۱]: اساس مبدلهای چندسطحی



**FIGURE 2.21** Line voltage waveforms for a three-phase diode-clamped inverter with three-level legs.

#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

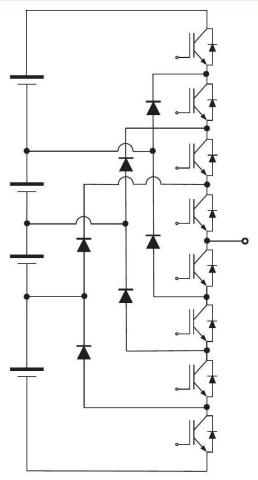
Here we emphasize the relationship between the number of levels in phase and line voltages:

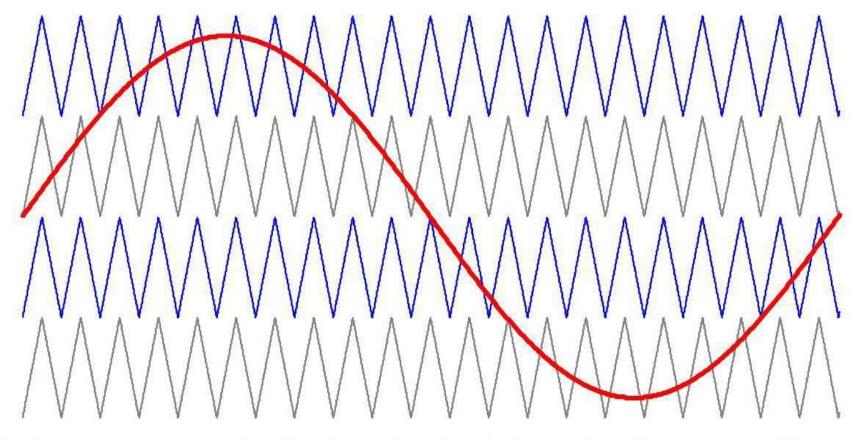
Number of levels in line voltage =  $2 \times (\text{number of levels in phase voltage}) - 1$  (2.4)

#### **\* 2.3.2 Diode-Clamped Structure and Modulation Strategies**

In order to extend the number of levels, the structure can be systematically extended. One such example is shown in Fig. 2.22 with a single leg. The reader is encouraged to determine working valid states for this structure and to see how the clamping diodes shown have unequal blocking voltage requirements. Similarly, for modulation of diode-clamped structures with a higher number of levels, the number of carrier signals can be increased with appropriate "level-shifting" as depicted in Fig. 2.23. Later chapters contain more discussions on modulation techniques.

√ فصل ۲ [۱]: اساس مبدلهای چندسطحی





**FIGURE 2.23** Multiple "level-shifted" carrier signals to obtain a five-level PWM waveform.

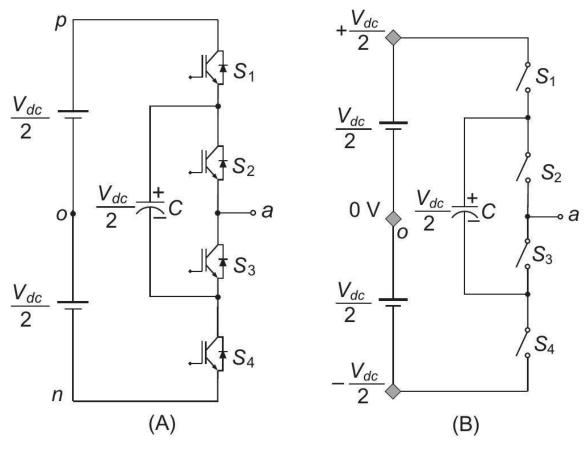
**2.3.3** Flying Capacitor Structure and Modulation Strategies

#### 2.3.3 FC Structure and Modulation Strategies

The so-called FC was introduced in the late 1980s [5, 6]. This topology does not use any clamping diodes. Instead it uses capacitors which are not directly connected to the positive or negative DC rails; hence the name "floating" or "flying" capacitor (FC) topology. A leg of three-level FC topology is shown in Fig. 2.24A.

۰ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.3 Flying Capacitor Structure and Modulation Strategies**



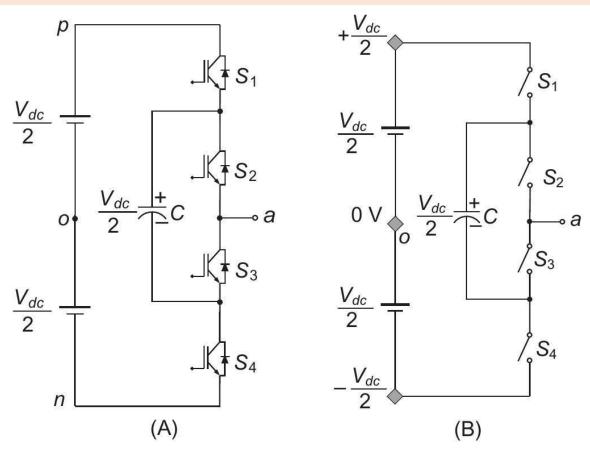
**FIGURE 2.24** (A) One leg of a three-level FC MLI; and (B) equivalent representation for the purposes of analysis.

#### **2.3.3** Flying Capacitor Structure and Modulation Strategies

As shown in Fig. 2.24A, the input voltage is  $V_{dc}$ , shown with two voltage sources of value  $V_{dc}/2$  each. The common point is marked as "o" and the load voltage is measured as the potential difference between points "a" and "o,"  $v_{ao}(t)$ . The structure has four bidirectional-conducting-unidirectional-blocking switches and one floating capacitor "C." The positive and negative DC rails are marked with "p" and "n," respectively. The floating capacitor "C" is "precharged" to a voltage  $V_{dc}/2$  with polarity as shown in Fig. 2.24A.

۷ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.3 Flying Capacitor Structure and Modulation Strategies**



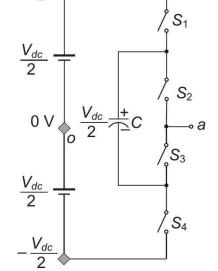
**FIGURE 2.24** (A) One leg of a three-level FC MLI; and (B) equivalent representation for the purposes of analysis.

√ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.3 Flying Capacitor Structure and Modulation Strategies**

The modulation scheme has to ensure proper maintenance of this voltage across the capacitor. For the purpose of analysis of this structure, an equivalent circuit with symbolic switches is shown in Fig. 2.24B. Point "o" is assumed to be the reference node with a potential of 0 V. Accordingly, the potentials at the positive and negative rails are  $+V_{dc}/2$  and  $-V_{dc}/2$ . There are four valid states summarized in Fig. 2.25.

B) equivalent representation for the purposes of analysis.



### √ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.3 Flying Capacitor Structure and Modulation Strategies**

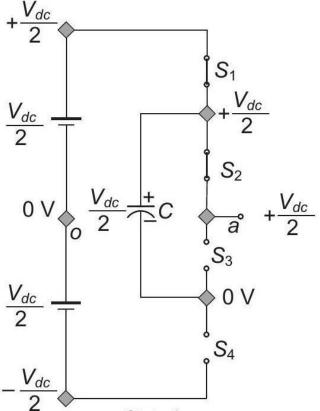
As can be observed from Fig. 2.25A, when  $S_1$  and  $S_2$  are simultaneously switched ON, a voltage of  $V_{dc}/2$  is obtained across the load, while the volt-

age stress across the blocking switches is  $V_{dc}/2$ .

#### State 1

- ·  $S_1$  and  $S_2$  are ON;  $S_3$  and  $S_4$  are OFF
- · Potential at  $a = +V_{DC}/2$
- $\cdot v_{ao}(t) = V_{DC}/2$
- · Voltage stress across  $S_3$  and  $S_4 = V_{DC}/2$

(A)



### √ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.3 Flying Capacitor Structure and Modulation Strategies**

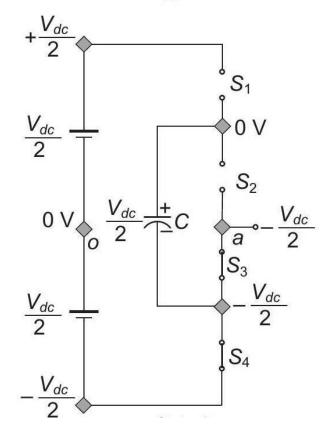
In State 2, when Switches  $S_3$  and  $S_4$  are simultaneously turned ON, a voltage of  $-V_{dc}/2$  appears across the load, while the voltage stress across

the blocking devices is  $V_{dc}/2$ .

#### State 2

- ·  $S_3$  and  $S_4$  are ON;  $S_1$  and  $S_2$  are OFF
- · Potential at  $a = -V_{DC}/2$
- $\cdot v_{ao}(t) = -V_{DC}/2$
- · Voltage stress across  $S_1$  and  $S_2 = V_{DC}/2$

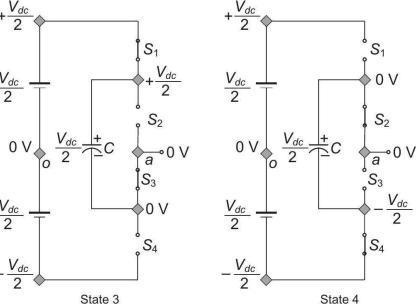
(B)



#### **\* 2.3.3 Flying Capacitor Structure and Modulation Strategies**

States 3 and 4, both lead to a load voltage of 0 V, although with different switching combinations, and hence they are redundant states. These redundant states are used to balance the capacitor voltages. As described earlier, the FC has to be precharged and voltages need to be balanced. Such switching procedures are discussed in later chapters, in which control is

heavily based on the state selection procedure.  $+\frac{V_{dc}}{2}$ 



#### √ فصل ۲ [۱]: اساس مبدلهای چندسطحی

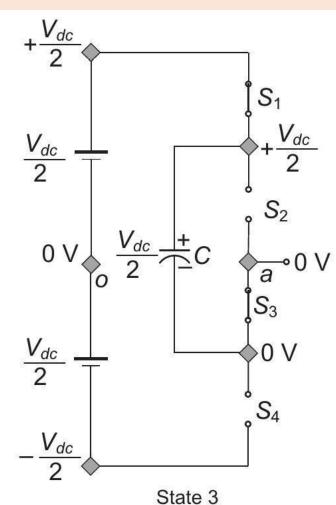
#### **\* 2.3.3 Flying Capacitor Structure and Modulation Strategies**

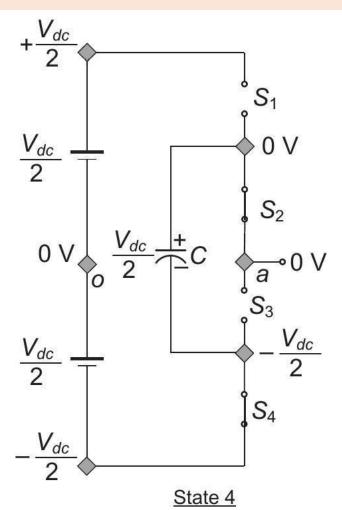
#### State 3

- ·  $S_1$  and  $S_3$  are ON;  $S_2$  and  $S_4$  are OFF
- · Potential at a = 0 V
- $v_{ao}(t) = 0$
- · Voltage stress across  $S_2$  and  $S_4 = V_{DC}/2$  (C)

#### State 4

- ·  $S_2$  and  $S_4$  are ON;  $S_1$  and  $S_3$  are OFF
- · Potential at a = 0 V
- $v_{ao}(t) = 0$
- · Voltage stress across  $S_1$  and  $S_3 = V_{DC}/2$  (D)



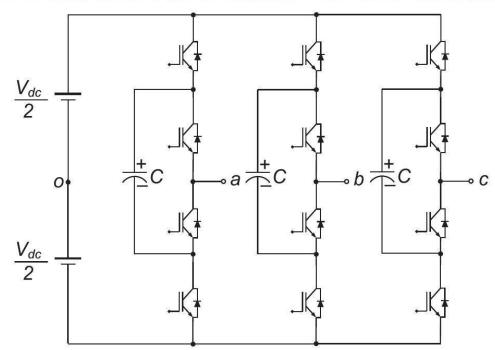


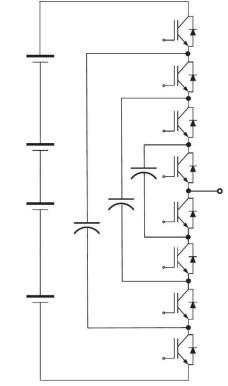
#### √ فصل ۲ [۱]: اساس مبدلهای چندسطحی

#### **\* 2.3.3 Flying Capacitor Structure and Modulation Strategies**

A three-phase inverter based on a three-level FC leg is shown in Fig. 2.26 and an extension of this topology is shown in Fig. 2.27. The reader

should work out the valid states for this structure.





٣۵

FIGURE 2.26 A three-phase FC topology with three-level legs.

#### **2.3.3** Flying Capacitor Structure and Modulation Strategies

While a more detailed discussion on modulation schemes is given in later chapters, it should be emphasized here that, in principle, any topology can be modulated with either a level-shifted or phase-shifted carrier-based methodology, when suitably adapted.

**\* 2.4 Issues with Conventional Topologies** 

#### 2.4 ISSUES WITH CONVENTIONAL TOPOLOGIES

The fundamentals of conventional/classical topologies were discussed in Section 2.3. These topologies have been commercialized, but they have certain issues. The CHB topology requires isolated DC sources and, in the case that these sources are not readily available (e.g., in the case of AC drives), transformers with multiple secondary windings are used along with a rectifier to obtain isolated DC levels. CHB topology, of course, is highly modular in nature. For the diode-clamped inverter, a single DC link works for all three phases. But, as the number of levels increases, voltage balancing in DC link capacitors becomes difficult.

#### **\* 2.4 Issues with Conventional Topologies**

Also, the switching frequencies are different for the switches of a leg, which leads to unequal lifetimes of these switches. Diode-clamped inverters, however, are highly suitable for back-to-back applications such as AC electric drives. In the case of FC topology, a single DC link is sufficient for three phases. Here too, for an increased number of levels, balancing voltages in DC link capacitors and in floating capacitors becomes difficult. In addition, the presence of a large number of capacitors puts a limit on the switching frequency.

#### **\* 2.4 Issues with Conventional Topologies**

In addition to these, there is a common issue with these topologies: for an increased number of levels, these topologies inadvertently require a large number of switches. Each power switch is accompanied by a gate driver unit and heat sink, hence the overall system becomes bulky and complex. This is *one* of the reasons behind the emergence of advanced topologies in the last few years. Detailed discussions on this will follow in later chapters.

#### **\* 2.4 Issues with Conventional Topologies**

#### 2.5 SUMMARY

In this chapter a simplified and systematic approach is used to introduce the concept of MLIs. In addition to explanation of the concept, popular terminology related to MLIs is also discussed where appropriate. A detailed account of the three classic topologies (namely, CHB, diode-clamped, and FC topologies) is presented. With the application to these topologies, an important introduction to multiple carriers-based multilevel PWM schemes is also presented in this chapter. Level-shifted carriers-based PWM is discussed with reference to diode-clamped topology, while phase-shifted carriers-based multilevel PWM is discussed with reference to the CHB topology.