روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

تعداد واحد: ۳ (نظری)

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پیش‌نیاز: -

هم‌نیاز: الکترونیک صنعتی

هدف: آشنایی با انواع روش‌های کنترلی انواع مبدل‌های dc-dc، dc-ac، ac-dc و ac-ac

- معرفی انواع شاخص‌های لازم در طراحی مبدل‌های الکترونیک قدرت
- معرفی پارامترهای کارآیی برای انواع مبدل‌های الکترونیک قدرت
- معرفی و نحوه پیاده‌سازی انواع روش‌های مدولاسیون بردار فضایی، تکنیک مدولاسیون پهنای پالس (PWM)، شیفت فاز، باند هیسترزیس برای کنترل انواع مبدل‌های الکترونیک قدرت در حالت‌های متقارن و نامتقارن
- معرفی و نحوه پیاده‌سازی انواع روش‌های کنترلی شارژ متعادل برای اینورترهای چندسطحی

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❑ مراجع

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[2] Gonzalez, S.A., Verne, S.A. and Valla, M.I., 2016. Multilevel converters for industrial applications. CRC Press.

[3] Du, S., Dekka, A., Wu, B. and Zargari, N., 2017. Modular multilevel converters: analysis, control, and applications. John Wiley & Sons.

فصل سوم [۱]

ظهور ساختارهای جدید

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3 MLI Topologies with Reduced Device Count

3.3 MLI TOPOLOGIES WITH REDUCED DEVICE COUNT

For the past few years, many researchers have been working on MLI topologies with a significant reduction in component count as compared to the classical topologies. Judging a topology without the consideration of the specific application is not only difficult, but also futile and unjustified. Often it can be seen that, while a topology is near-perfect for one application, it is useless for another. Still, in the context of this book, the general criteria for an overall assessment of a topology include:

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❖ 3.3 MLI Topologies with Reduced Device Count

1. the number of power switches used;
2. the total blocking voltage of the converter (which depends on the number of power switches and their respective voltage ratings);
3. the optimal controllability of the topology (in terms of possibility of charge-balance control and switching of the differently rated switches); and
4. possibility of employing asymmetric sources/capacitor voltage ratios.

While Parameters (1) and (2) directly influence the reliability of the inverter, efficiency is influenced by Parameters (1), (2), and (3) and application, performance and control complexity are governed by Parameter (3). The number of redundant states and consequently the programmability of fault-tolerant operation is directly influenced by (1) and (4). Based on these parameters, topologies with reduced component counts are discussed in this section.

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.1 Cascaded Half-Bridge-Based Multilevel DC Link Inverter

3.3.1 Cascaded Half-Bridge-Based Multilevel DC Link Inverter

Gui-Jia [58,59] introduced a new class of MLIs based on a multilevel DC link (MLDCL) and a bridge inverter to reduce the device count. An MLDCL, as shown in Fig. 3.1, has cascaded half-bridge cells with each cell having its own DC source. A multilevel voltage-source inverter can be formed by connecting one of the MLDCLs with a single-phase bridge inverter. The MLDCL, which is comprised of sources $V_{DC,j}$ $\{j = 1-3\}$ and power switches S_j $\{j = 1-6\}$, generates a stepped waveform with one polarity, with or without PWM, to the bridge inverter, comprised of switches Q_j $\{j = 1-4\}$, which in turn alternates the polarity to produce an alternating voltage.

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.1 Cascaded Half-Bridge-Based Multilevel DC Link Inverter

For an increased number of levels at the output, the MLDCL inverter can significantly reduce the switch count as well as the number of gate drivers as compared to the CHB topology [58]. With reference to Fig. 3.1, various combinations that can be obtained for the MLDCL v_{bus} are summarized in Table 3.1.

It can be observed that, to obtain a given level, three switches conduct simultaneously in the MLDCL part and two switches conduct in the H-bridge part (Switches Q_1 and Q_4 for the positive half cycle, Q_2 and Q_3 for the negative half cycle, and Q_1 and Q_3 or Q_2 and Q_4 for zero level).

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.1 Cascaded Half-Bridge-Based Multilevel DC Link Inverter

TABLE 3.1 Switching States for the Topology Shown in Fig. 3.1

State	Multilevel DC Link Bus Voltage v_{bus}	Switches in ON State
1	$V_{DC,1}$	S_2, S_3, S_5
2	$V_{DC,2}$	S_1, S_4, S_5
3	$V_{DC,3}$	S_1, S_3, S_6
4	$V_{DC,1} + V_{DC,2}$	S_2, S_4, S_5
5	$V_{DC,2} + V_{DC,3}$	S_1, S_4, S_6
6	$V_{DC,1} + V_{DC,3}$	S_2, S_3, S_6
7	$V_{DC,1} + V_{DC,2} + V_{DC,3}$	S_2, S_4, S_6
8	0	S_1, S_3, S_5

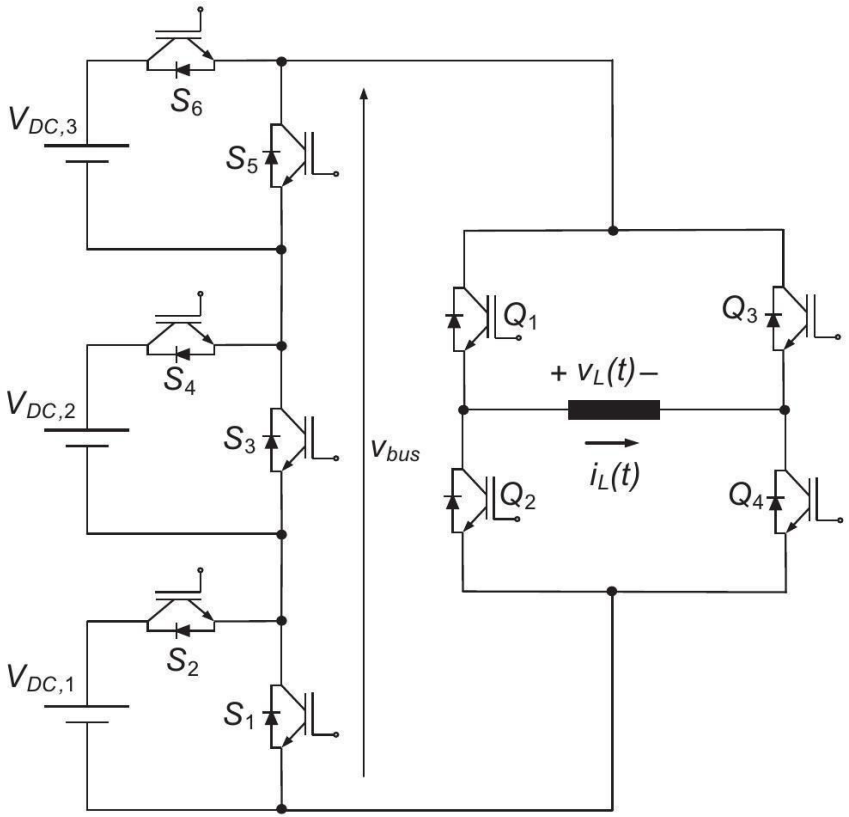

FIGURE 3.1 MLDCL inverter.

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.1 Cascaded Half-Bridge-Based Multilevel DC Link Inverter

It can
be observed from the topology that each power switch of the H-bridge part must have a minimum voltage-blocking capability equal to the sum of the input voltage values. Thus, these switches are rated higher compared to the switches in the MLDCL part. However, since the zero level can be synthesized using switches of the MLDCL part, the higher-rated switches Q_j $\{j = 1-4\}$ can be operated at fundamental switching frequency.

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.1 Cascaded Half-Bridge-Based Multilevel DC Link Inverter

For a symmetric source configuration with $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC}$, it can be seen that the switches S_j $\{j = 1-6\}$ need to block a voltage of V_{DC} and need to conduct a current equal to the load current. Switches Q_j $\{j = 1-4\}$ need to block a voltage equal to $3V_{DC}$ and conduct a current equal to the load current. It can also be observed from Table 3.1 that since voltage levels V_{DC}, $2V_{DC}$, and $3V_{DC}$ can be synthesized combining all the input sources in groups of one, two, and three, respectively, equal load sharing amongst them is possible. These redundancies also provide flexibility in voltage balancing when capacitors are used.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.1 Cascaded Half-Bridge-Based Multilevel DC Link Inverter

Regarding asymmetric source configurations in MLDCL topology, no analysis is offered in References [58,59]. Since subtractive combinations of the input DC levels cannot be synthesized, the trinary source configuration (i.e., $V_{DC,\,j} = 3^{(j-1)}\ V_{DC}$) cannot be employed for this topology. As can be seen from Table 3.1, a binary combination with $V_{DC,1} = V_{DC}$, $V_{DC,2} = 2V_{DC}$ and $V_{DC,3} = 4V_{DC}$ is possible since the voltage levels V_{DC}, $2V_{DC}$, $3V_{DC}$, $4V_{DC}$, $5V_{DC}$, $6V_{DC}$, and $7V_{DC}$ can be synthesized by using States 1, 2, 4, 3, 6, 5, and 7, respectively.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.2 T-Type Inverter

3.3.2 T-Type Inverter

Gerardo Ceglia et al. [60–62] have presented a new MLI topology, named the T-type inverter, comprising an H-bridge output stage and bidirectional auxiliary switches. It offers a significant reduction in the number of power devices as compared to conventional topologies. A single-phase structure with four input voltage sources, namely, $V_{DC,1}$, $V_{DC,2}$, $V_{DC,3}$, and $V_{DC,4}$, is shown in Fig. 3.2. It comprises three switches S_j $\{j = 1–3\}$ which are bidirectional-blocking-bidirectional-conducting, while four switches Q_j $\{j = 1–4\}$ are unidirectional-blocking-bidirectional-conducting.

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.2 T-Type Inverter

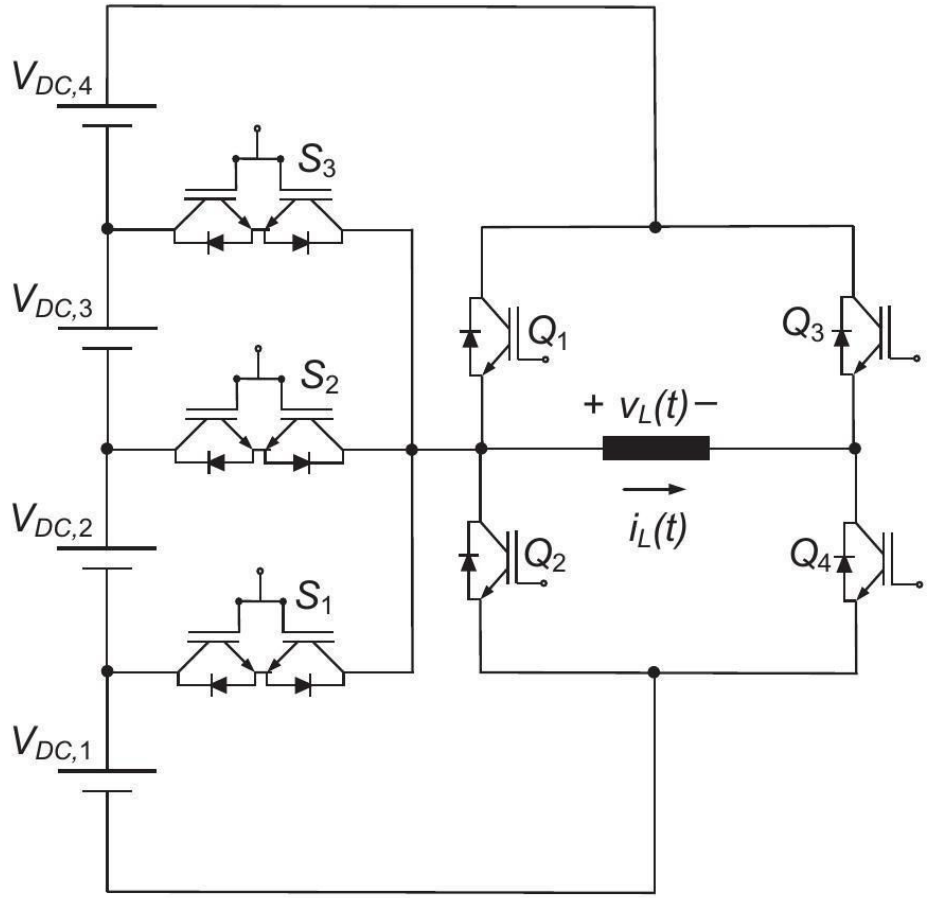

FIGURE 3.2 A T-type inverter with four input sources.

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.2 T-Type Inverter

Thus, this topology inadvertently requires a mix of unidirectional and bidirectional power switches. The valid switching states are summarized in Table 3.2 and it can be seen that the input DC values are required to be symmetric, i.e., $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$. This is because not all combinations of input voltage levels can be synthesized at the load terminals. In most cases, either a positive or negative combination can be synthesized, but not both.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.2 T-Type Inverter

For example, while a voltage level $-V_{DC,4}$ can be synthesized at the load terminals, the level $+V_{DC,4}$ cannot be synthesized. Thus, it is essential that the input sources are symmetric. Also, lack of sufficient redundancies goes against effective voltage balancing. It can be also observed from Table 3.2 that equal load sharing amongst the input voltage sources is not possible as the number of valid states is very limited. For a given state, only two switches conduct simultaneously. The bidirectional switches are voltage-rated at different values. While S_3 should be minimally rated at $3V_{DC}$, S_2 and S_1 should be rated at $2V_{DC}$ each. The H-bridge switches must each have minimum blocking capability of $4V_{DC}$. These higher voltage switches, however, can be operated with fundamental switching frequency.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.2 T-Type Inverter

TABLE 3.2 Possibilities of Switching Combinations for the Topology Shown in Fig. 3.2

State	Output Voltage $v_L(t)$	Switches in ON State (Other Switches Remain OFF)
1	$+V_{DC,1}$	S_1, Q_4
2	$-V_{DC,1}$	Not possible
3	$+V_{DC,2}$	Not possible
4	$-V_{DC,2}$	Not possible
5	$+V_{DC,3}$	Not possible
6	$-V_{DC,3}$	Not possible
7	$+V_{DC,4}$	Not possible
8	$-V_{DC,4}$	S_3, Q_3
9	$V_{DC,1}+V_{DC,2}$	S_2, Q_4

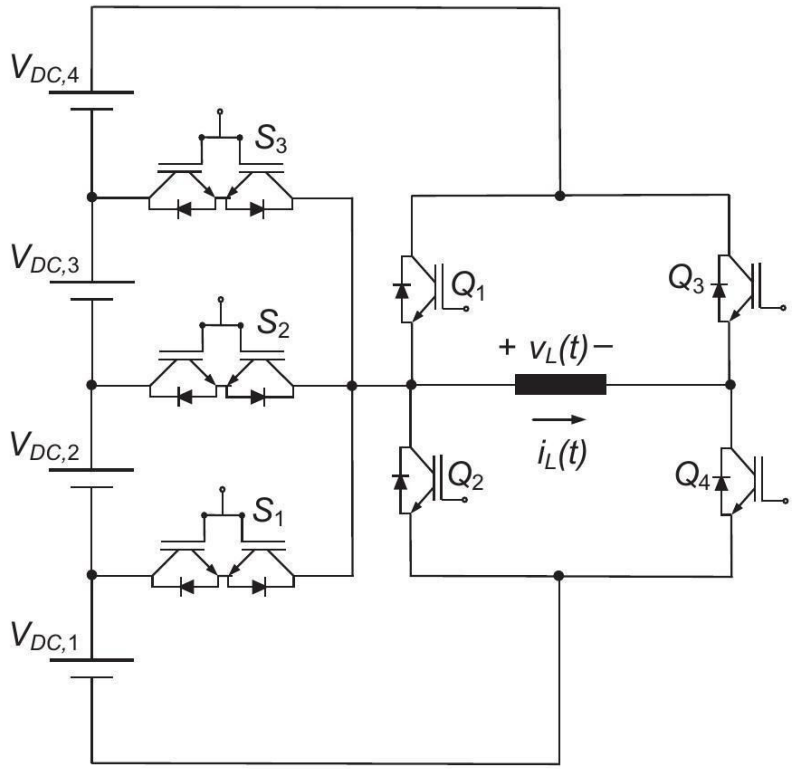

FIGURE 3.2 A T-type inverter with four input sources.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.2 T-Type Inverter

TABLE 3.2 Possibilities of Switching Combinations for the Topology Shown in Fig. 3.2

State	Output Voltage $v_L(t)$	Switches in ON State (Other Switches Remain OFF)
10	$-(V_{DC,1} + V_{DC,2})$	Not possible
11	$V_{DC,2} + V_{DC,3}$	Not possible
12	$-(V_{DC,2} + V_{DC,3})$	Not possible
13	$V_{DC,3} + V_{DC,4}$	Not possible
14	$-(V_{DC,3} + V_{DC,4})$	S_2, Q_3
15	$V_{DC,1} + V_{DC,3}$	Not possible
16	$-(V_{DC,1} + V_{DC,3})$	Not possible
17	$V_{DC,1} + V_{DC,4}$	Not possible
18	$-(V_{DC,1} + V_{DC,4})$	Not possible
19	$V_{DC,2} + V_{DC,4}$	Not possible

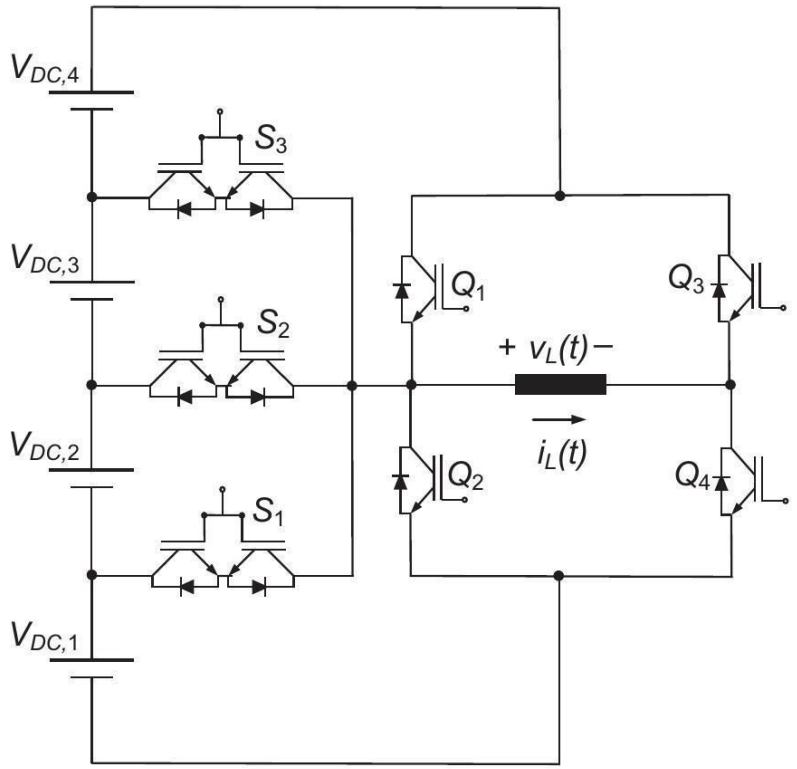

FIGURE 3.2 A T-type inverter with four input sources.

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.2 T-Type Inverter

TABLE 3.2 Possibilities of Switching Combinations for the Topology Shown in Fig. 3.2

State	Output Voltage $v_L(t)$	Switches in ON State (Other Switches Remain OFF)
20	$-(V_{DC,2}+V_{DC,4})$	Not possible
21	$V_{DC,1}+V_{DC,2}+V_{DC,3}$	S_3, Q_4
22	$-(V_{DC,1}+V_{DC,2}+V_{DC,3})$	Not possible
23	$V_{DC,2}+V_{DC,3}+V_{DC,4}$	Not possible
24	$-(V_{DC,2}+V_{DC,3}+V_{DC,4})$	S_1, Q_3
25	$V_{DC,1}+V_{DC,2}+V_{DC,4}$	Not possible
26	$-(V_{DC,1}+V_{DC,2}+V_{DC,4})$	Not possible
27	$V_{DC,1}+V_{DC,3}+V_{DC,4}$	Not possible
28	$-(V_{DC,1}+V_{DC,3}+V_{DC,4})$	Not possible

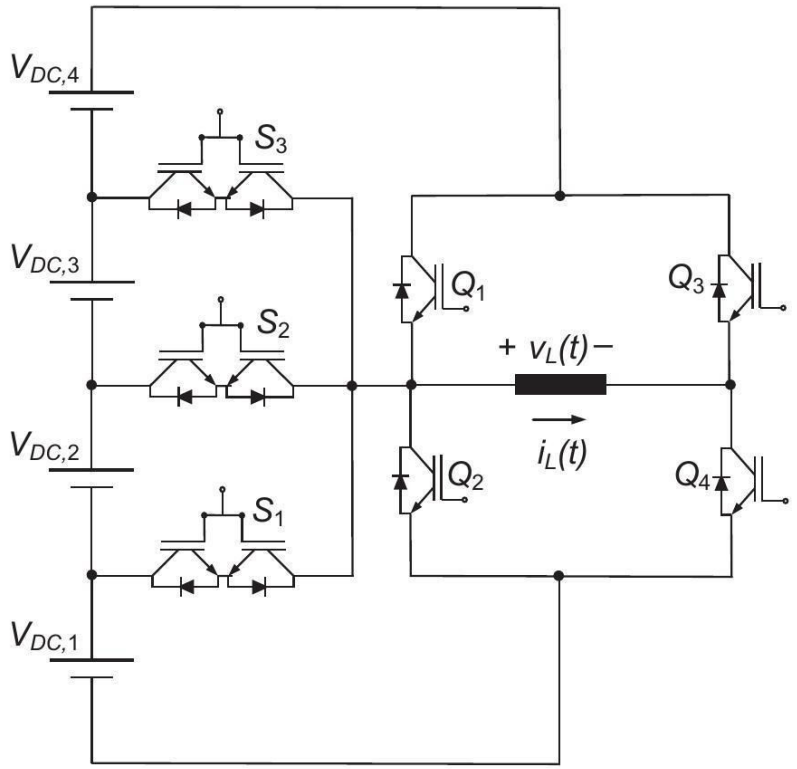

FIGURE 3.2 A T-type inverter with four input sources.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.2 T-Type Inverter

TABLE 3.2 Possibilities of Switching Combinations for the Topology Shown in Fig. 3.2

State	Output Voltage $v_L(t)$	Switches in ON State (Other Switches Remain OFF)
29	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4}$	Q_1, Q_4
30	$-(V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4})$	Q_2, Q_3
31	0	Q_1, Q_3
32	0	Q_2, Q_4

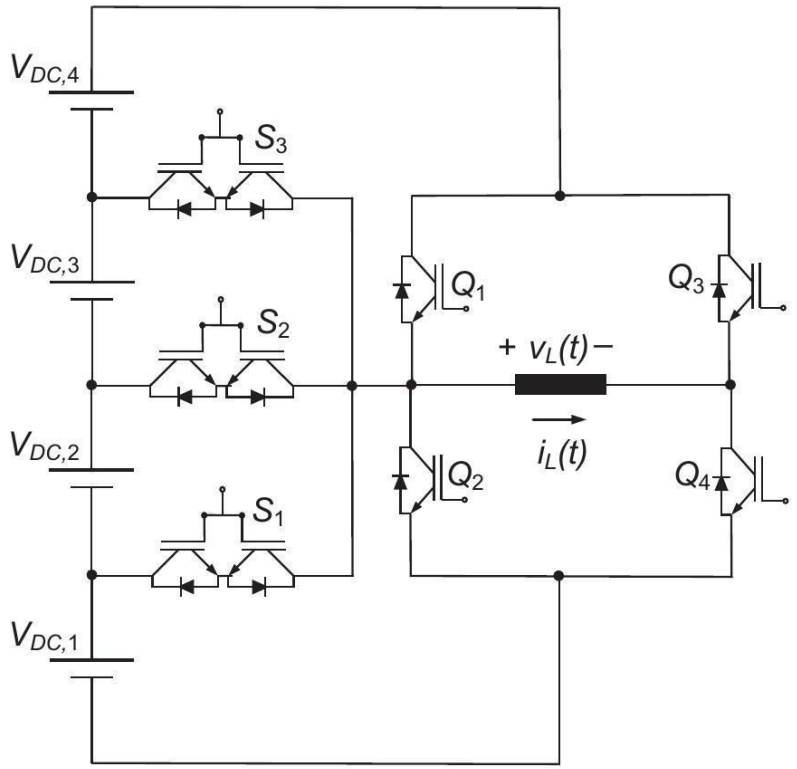

FIGURE 3.2 A T-type inverter with four input sources.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.3 Switched Series/Parallel Sources-Based MLI

3.3.3 Switched Series/Parallel Sources–Based MLI

Hinago and Koizumi [63,64] have proposed an MLI topology consisting of an H-bridge and DC sources which can be switched in series and in parallel. The topology reduces the number of gate driver circuits, thereby reducing the size and power consumption. The topology synthesizes the same number of output levels with a lower number of power switches as compared to a CHB topology. An important suggested application is for electric vehicular applications where a single battery composed of a number of series-connected battery cells is available, which can be rearranged using the switched sources topology, hence reducing the requirement for switching devices.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.3 Switched Series/Parallel Sources-Based MLI

More importantly, the possibility of combining two or more sources in series and parallel gives enough flexibility for meeting voltage/power requirements in the vehicle drive system.

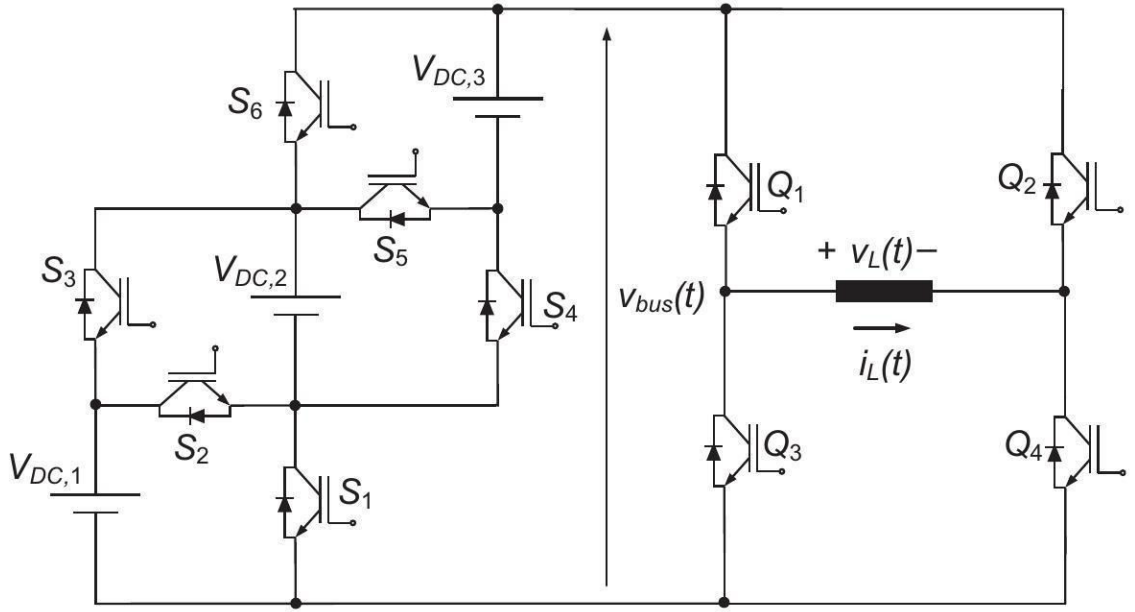

FIGURE 3.3 MLI topology as proposed in References [63,64].

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.3 Switched Series/Parallel Sources-Based MLI

An Switched Series/Parallel Sources−MLI with three input DC sources is shown in Fig. 3.3. It consists of two parts: the switched sources part which synthesizes a bus voltage $v_{bus}\ (t)$ and the H-bridge part which synthesizes positive and negative cycles of voltage $v_{bus}\ (t)$ to feed an AC load. Three sources, namely, $V_{DC,1}$, $V_{DC,2}$, and $V_{DC,3}$ and power switches $S_j\ \{j = 1-6\}$ constitute the switched sources part. Power switches $Q_j\ \{j = 1-4\}$ constitute the H-bridge part. Levels that can be synthesized by the switched sources part are summarized in Table 3.3.

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.3 Switched Series/Parallel Sources-Based MLI

For a symmetric source configuration, i.e., $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC}$, it can be seen from Table 3.3 that voltage levels V_{DC} and $2V_{DC}$ can be synthesized with three states each, while one state is available for voltage level $3V_{DC}$. Moreover, the voltage stress experienced by the switches S_j $\{j = 1-6\}$ would each be equal to V_{DC}. An important limitation of this topology is that the switches Q_j $\{j = 1-4\}$ need to have a minimum blocking capability of summation of voltages of all voltage sources. Thus, for the symmetric source configuration with three sources, the H-bridge switches should possess a voltage-blocking capability of $3V_{DC}$. Another important limitation is that these switches with higher blocking capability cannot be operated at fundamental switching frequencies because the zero voltage level is not synthesized by the switched sources part, as can be observed from Table 3.3.

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.3 Switched Series/Parallel Sources-Based MLI

TABLE 3.3 Switching States for Topology Shown in Fig. 3.3

State	Bus Voltage $v_{bus}(t)$	Switches in ON State
1	$V_{DC,1}$	S_3, S_6
2	$V_{DC,2}$	S_1, S_6
3	$V_{DC,3}$	S_1, S_4
4	$V_{DC,1} + V_{DC,2}$	S_2, S_6
5	$V_{DC,2} + V_{DC,3}$	S_1, S_5
6	$V_{DC,1} + V_{DC,3}$	S_3, S_5
7	$V_{DC,1} + V_{DC,2} + V_{DC,3}$	S_2, S_5

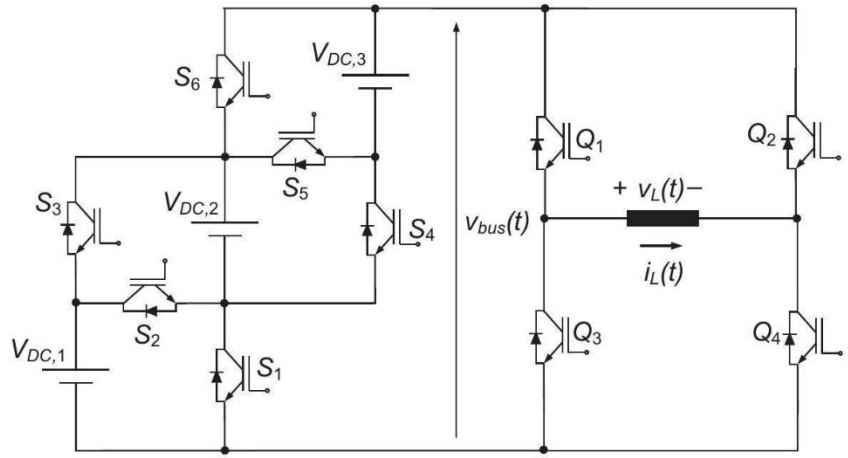

FIGURE 3.3 MLI topology as proposed in References [63,64].

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✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.3 Switched Series/Parallel Sources-Based MLI

can also be inferred from the table that, with input sources of equal voltages, equal load sharing amongst them is possible as the sources can be combined in all additive configurations. Various combinations can be utilized in different cycles so as to equate the average current from each source, thereby equalizing the average power amongst the sources.

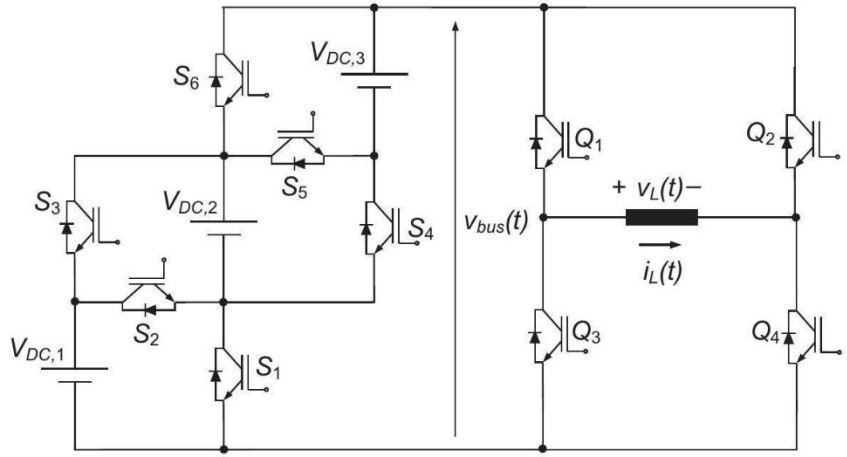


FIGURE 3.3 MLI topology as proposed in References [63,64].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.3 Switched Series/Parallel Sources-Based MLI

Although the topology enables the synthesis of all additive combinations of the input sources, subtractive combinations are not possible. Hence, trinary source configuration is not possible for this topology. Binary source configuration is, however, possible so as to maximize the number of levels in the output waveform. For example, in Fig. 3.3, for $V_{DC,1} = V_{DC}$, $V_{DC,2} = 2V_{DC}$, and $V_{DC,3} = 4V_{DC}$, all possible combinations, namely, V_{DC}, $2V_{DC}$, $3V_{DC}$, $4V_{DC}$, $5V_{DC}$, $6V_{DC}$, and $7V_{DC}$ are obtained as $v_{bus}(t)$ by using States 1, 2, 4, 3, 6, 5, and 7, so that the load voltage waveform has 15 levels in equal steps of V_{DC}. Thus, binary, but not trinary, source configuration can be implemented using this topology.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.4 Series-Connected Switched Sources-Based MLI

3.3.4 Series-Connected Switched Sources–Based MLI

A modified form of CHB topology is presented in References [65,66], with the objective of reducing the number of switches as compared to the classical CHB topology. The topology with four input DC sources $V_{DC,\,j}$ $\{j = 1–4\}$ is shown in Fig. 3.4. The low potential terminals of the sources are all connected through power switches. These terminals are also connected to the higher potential terminal of the preceding source through power switches, as illustrated in Fig. 3.4 with S_j $\{j = 1–8\}$. This interconnection is capable of synthesizing a multilevel rectified waveform v_{bus} which is imparted positive and negative polarities using the H-bridge comprising switches Q_j $\{j = 1–4\}$.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.4 Series-Connected Switched Sources-Based MLI

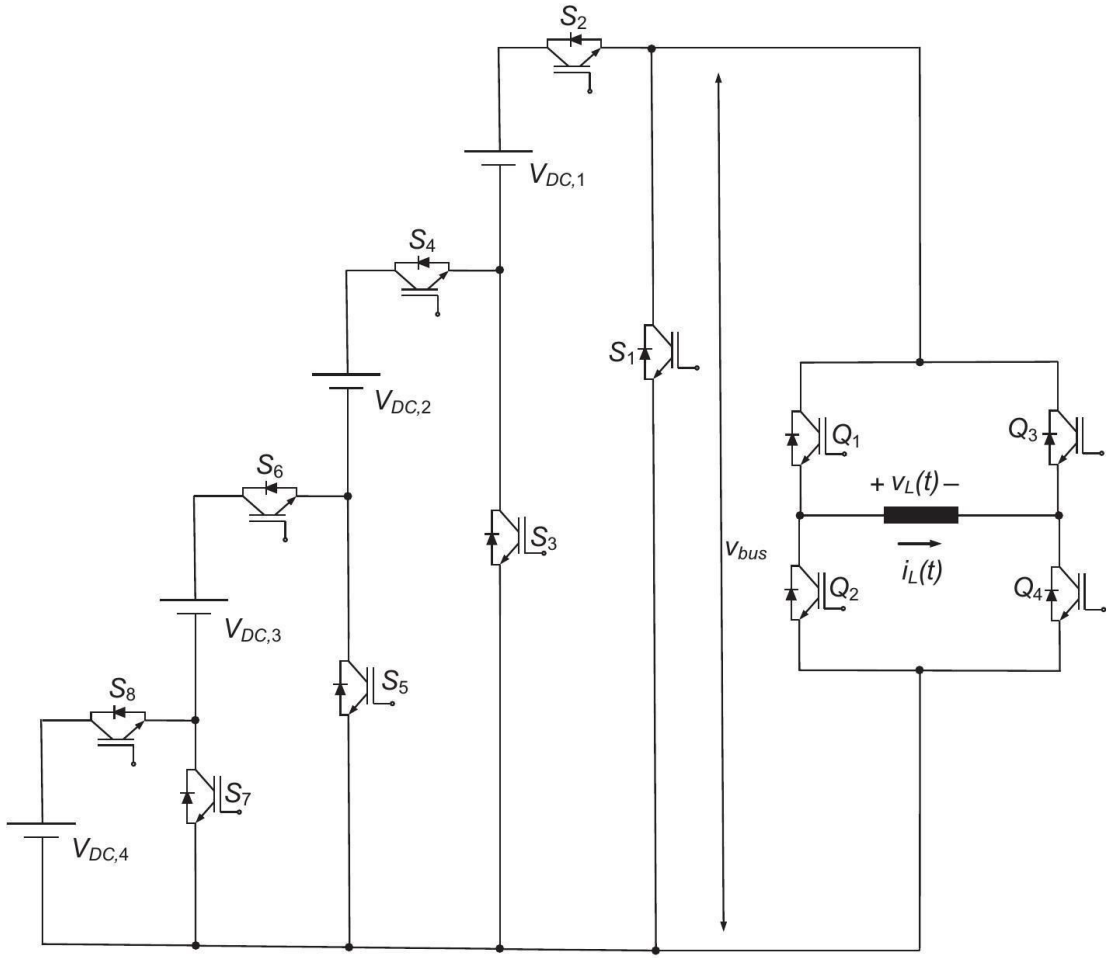


FIGURE 3.4 MLI topology as proposed in References [65,66].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.4 Series-Connected Switched Sources-Based MLI

The possibilities of synthesizing various combinations of input DC levels are summarized in Table 3.4. It can be seen that the structure, though simple, allows a much lower number of valid states. In fact, not even the input DC levels offered by the sources can all be obtained as v_{bus}, except that of $V_{DC,1}$.

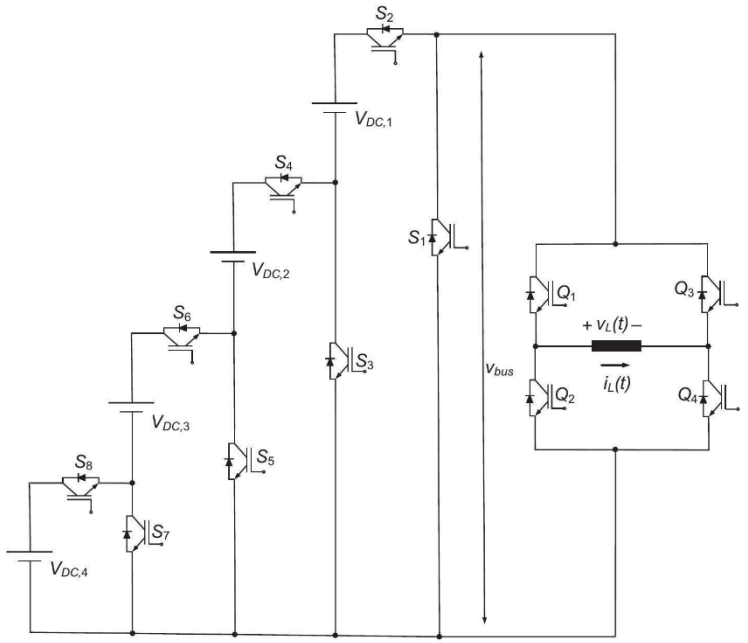


FIGURE 3.4 MLI topology as proposed in References [65,66].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.4 Series-Connected Switched Sources-Based MLI

TABLE 3.4 Possibilities of Switching Combinations for the Topology Shown in Fig. 3.4

State	Voltage Level v_{bus}	Switches in ON State
1	$V_{DC,1}$	S_1
2	$V_{DC,2}$	Not possible
3	$V_{DC,3}$	Not possible
4	$V_{DC,4}$	Not possible
5	$V_{DC,1} + V_{DC,2}$	S_2, S_3
6	$V_{DC,2} + V_{DC,3}$	Not possible
7	$V_{DC,3} + V_{DC,4}$	Not possible
8	$V_{DC,1} + V_{DC,4}$	Not possible
9	$V_{DC,2} + V_{DC,4}$	Not possible
10	$V_{DC,1} + V_{DC,3}$	Not possible
11	$V_{DC,1} + V_{DC,2} + V_{DC,3}$	S_2, S_4, S_5
12	$V_{DC,2} + V_{DC,3} + V_{DC,4}$	Not possible
13	$V_{DC,1} + V_{DC,3} + V_{DC,4}$	Not possible
14	$V_{DC,1} + V_{DC,2} + V_{DC,4}$	Not possible
15	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4}$	S_2, S_4, S_6
16	0	S_1

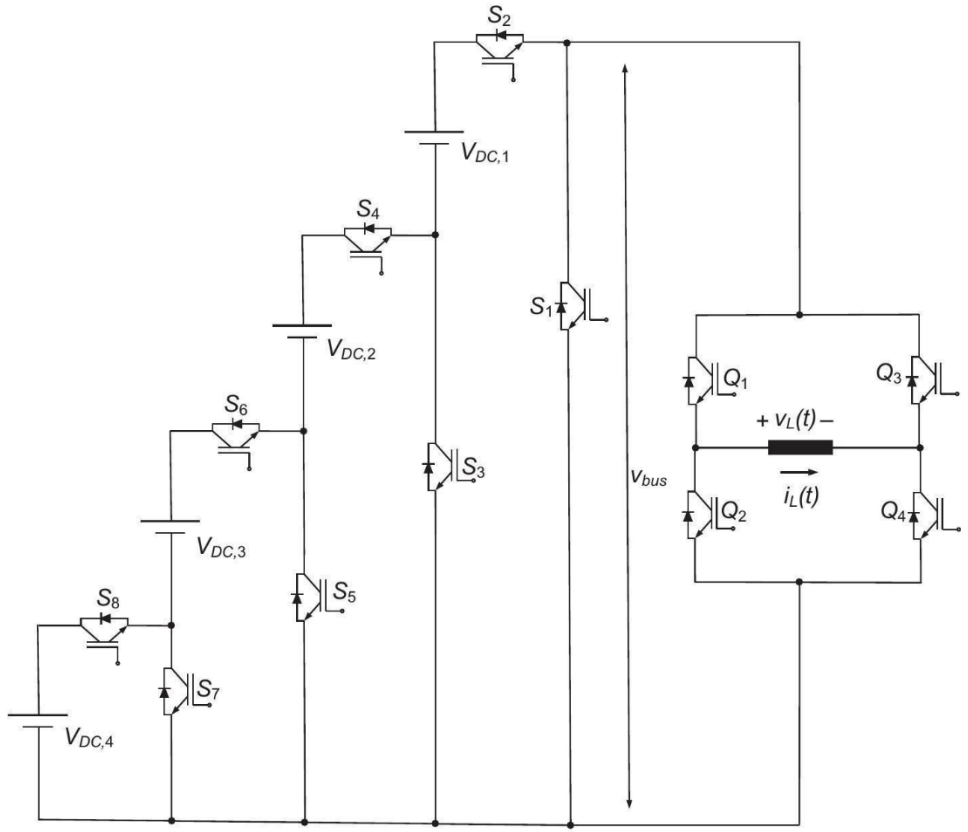


FIGURE 3.4 MLI topology as proposed in References [65,66].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.5 Cascaded “Bipolar Switches Cells”-Based MLI

3.3.5 Cascaded “Bipolar Switches Cells”—Based MLI

Babaei et al. [67] have presented a new class of multilevel converters to reduce the number of power electronics switches and DC voltage sources.

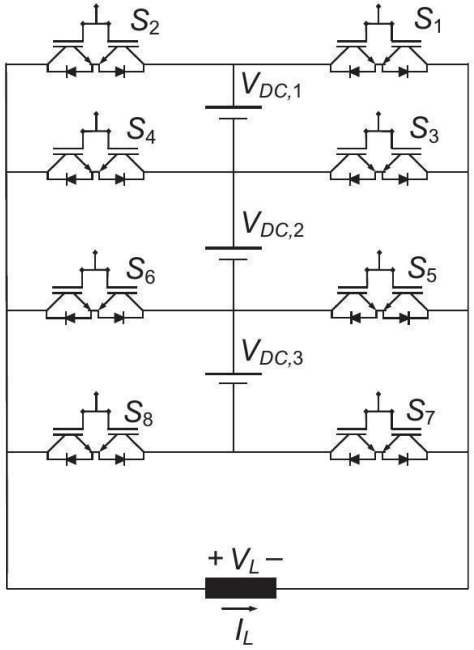


FIGURE 3.5 MLI topology as proposed in Reference [67].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.5 Cascaded “Bipolar Switches Cells”-Based MLI

Fig. 3.5 shows the single-phase structure of a seven-level converter with three input voltage sources with equal voltages of V_{DC} (symmetrical source configuration). All the switches are bidirectional-blocking-bidirectional-conducting. Although each bidirectional switch requires two IGBTs, the total number of gate drive circuits is equal to the number of bidirectional switches. This results in reducing the cost and overall complexity of the converter.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.5 Cascaded “Bipolar Switches Cells”-Based MLI

Switching states for all possible combinations of input voltage sources are shown in Table 3.5. It can be observed that while synthesizing $2V_{DC}$ and $-2V_{DC}$, not all possible combinations of input voltage sources are utilized. As a result, equal utilization of the input voltage sources is not possible in this topology. Moreover, the outermost bidirectional switches S_1, S_2, S_7, and S_8 need to have minimum voltage blocking capability of $3V_{DC}$ each. On the other hand, the inner switches S_3, S_4, S_5, and S_6 need to have minimum voltage blocking capability of $2V_{DC}$. It can also be observed that to synthesize each voltage level, only two switches need to conduct simultaneously. It should also be noted that the topology can only work with symmetrical sources configuration.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.5 Cascaded “Bipolar Switches Cells”-Based MLI

TABLE 3.5 Possibilities of Switching Combinations for the Topology Shown in Fig. 3.5

State	Output Voltage $V_L(t)$	Switches in ON State (Other Switches Remain OFF)	Remarks
1	$V_{DC,1}$	S_2, S_3	
2	$V_{DC,2}$	S_4, S_5	
3	$V_{DC,3}$	S_6, S_7	
4	$V_{DC,1} + V_{DC,2}$	S_2, S_5	
5	$V_{DC,2} + V_{DC,3}$	S_4, S_7	
6	$V_{DC,3} + V_{DC,1}$	S_2, S_3, S_5, S_7	Not possible as $V_{DC,2}$ gets short-circuited
7	$V_{DC,1} + V_{DC,2} + V_{DC,3}$	S_2, S_7	

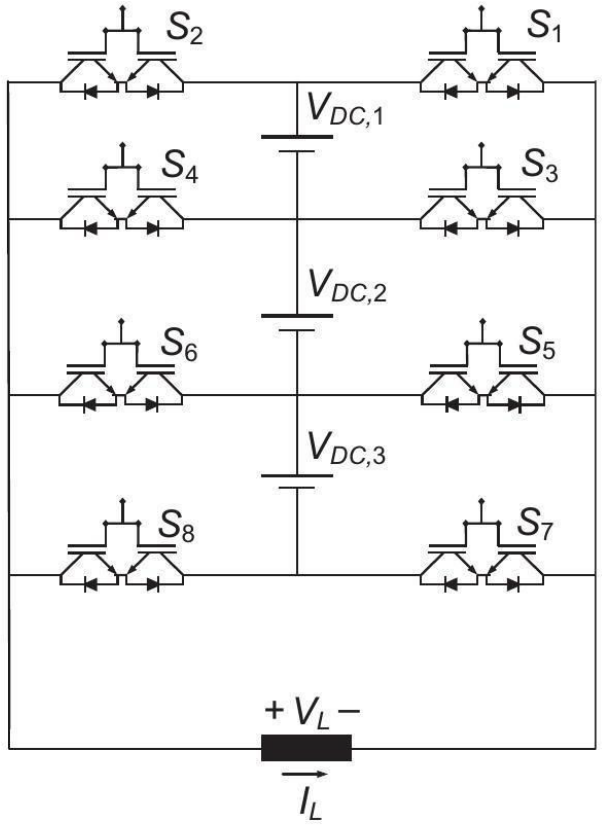


FIGURE 3.5 MLI topology as proposed in Reference [67].

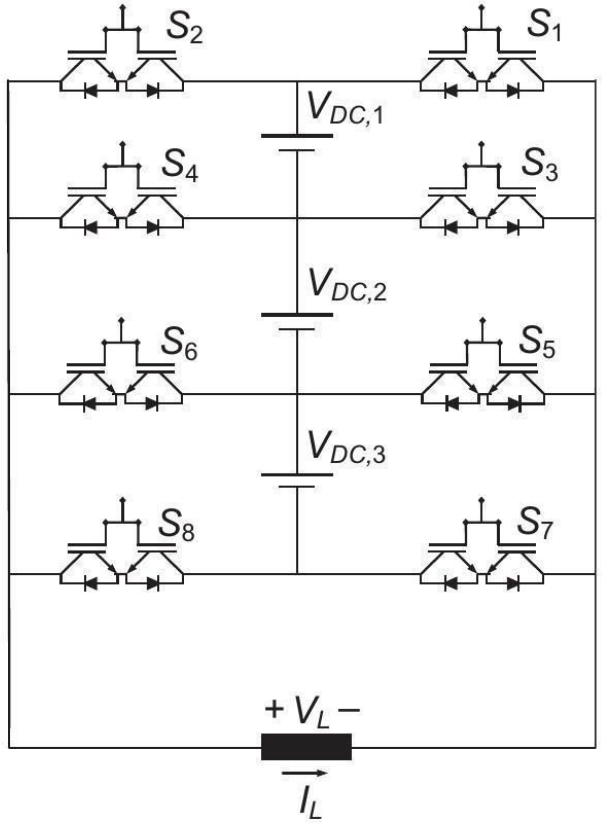
روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.5 Cascaded "Bipolar Switches Cells"-Based MLI

TABLE 3.5 Possibilities of Switching Combinations for the Topology Shown in Fig. 3.5

State	Output Voltage $V_L(t)$	Switches in ON State (Other Switches Remain OFF)	Remarks
8	$-V_{DC,1}$	S_1, S_4	
9	$-V_{DC,2}$	S_3, S_6	
10	$-V_{DC,3}$	S_5, S_8	
11	$-(V_{DC,1}+V_{DC,2})$	S_1, S_6	
12	$-(V_{DC,2}+V_{DC,3})$	S_3, S_8	
13	$-(V_{DC,3}+V_{DC,1})$	S_1, S_4, S_6, S_8	Not possible as $V_{DC,2}$ gets short-circuited
14	$-(V_{DC,1}+V_{DC,2}+V_{DC,3})$	S_1, S_8	
15	0	S_7, S_8	



3.5 MLI topology as proposed in Reference [67].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.6 Packed U-Cell Topology

3.3.6 Packed U-Cell Topology

Youssef Ounejjar et al. [68–72] have proposed a new topology which is very competitive compared to the classical topologies. It consists of the so-called "packed U cells." Each U cell consists of an arrangement of two power switches and one DC input level (obtained with a voltage source or a floating capacitor). A single-phase structure of the packed U-cell (PUC) topology with two input DC levels, namely, $V_{DC,1}$ and $V_{DC,2}$, and six switches S_j $\{j = 1–6\}$, is shown in Fig. 3.6.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.6 Packed U-Cell Topology

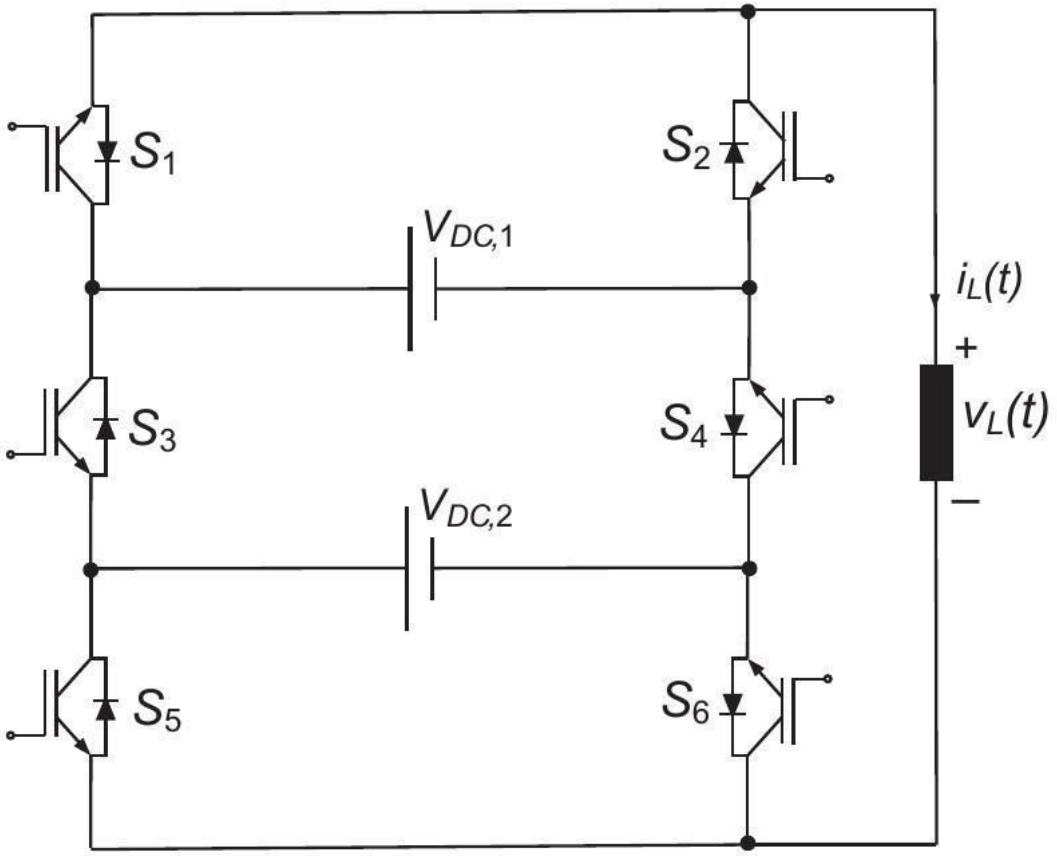


FIGURE 3.6 PUC MLI topology as proposed in References [68–72].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.6 Packed U-Cell Topology

The topology is very simple in terms of the interconnection of components. The minimum voltage-blocking capability required for switches (S_1, S_2) is $V_{DC,1}$, while that for (S_5, S_6) is $V_{DC,2}$. The voltage-blocking capability for switches (S_3, S_4) is ($V_{DC,1} - V_{DC,2}$). Various states for the structure are shown in Table 3.6. Thus, to obtain a desired voltage level, only three switches conduct simultaneously. It is important to observe from Table 3.6 that to derive the desired benefit from the topology, symmetric source configuration cannot be used as the output will be three-level with many redundant states.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.6 Packed U-Cell Topology

TABLE 3.6 Switching States for Topology Shown in Fig. 3.6

State	Output Voltage $v_L(t)$	Switches in ON State (Other Switches Remain OFF)
1	0	S_1, S_3, S_5
2	0	S_2, S_4, S_6
3	$V_{DC,1}$	S_1, S_4, S_6
4	$V_{DC,2}$	S_1, S_3, S_6
5	$V_{DC,1} - V_{DC,2}$	S_1, S_4, S_5
6	$-V_{DC,1}$	S_2, S_3, S_5
7	$-V_{DC,2}$	S_2, S_4, S_5
8	$-V_{DC,1} + V_{DC,2}$	S_2, S_3, S_6

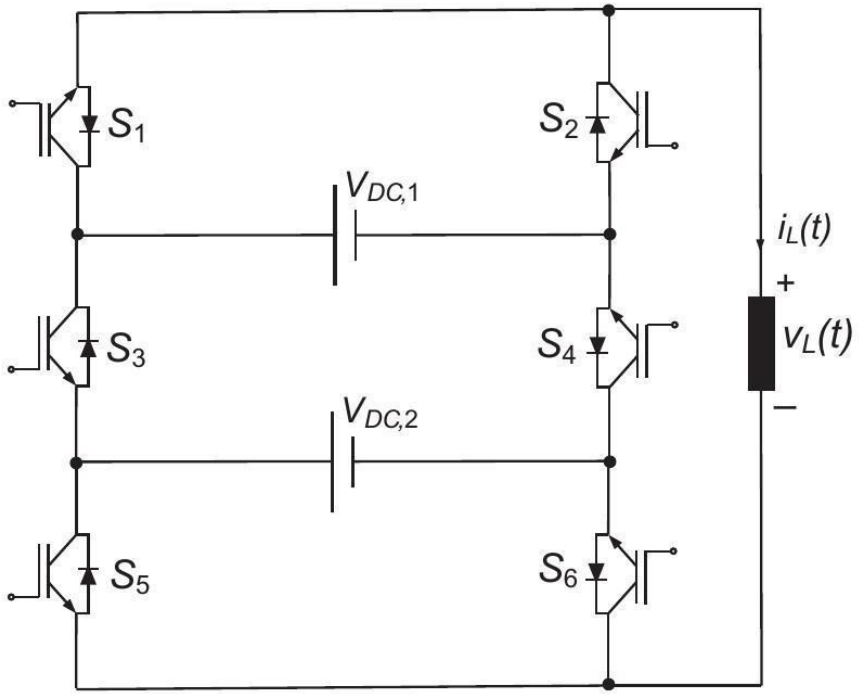


FIGURE 3.6 PUC MLI topology as proposed in References [68–72].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.6 Packed U-Cell Topology

An elaborate methodology is presented in Reference [72] to calculate the asymmetric voltage levels. For two input levels, the number of output levels can be maximized with $V_{DC,1} = 3V_{DC}$ and $V_{DC,2} = V_{DC}$. This trinary configuration synthesizes seven levels, not nine, because of the absence of additive combination. For a structure with two input sources, switching of the middle two switches, namely (S_3, S_4), can be performed at a fundamental frequency as demonstrated in Reference [72]. This feature, however, is not feasible for PUC-based structures with more than two input DC levels.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.7 Multilevel Module-Based MLI

3.3.7 Multilevel Module–Based MLI

The topology presented in Reference [73] also aims to reduce the number of switches. This topology is a hybrid multilevel topology comprising of two parts. The "level generation part" consists of input DC sources and bidirectional-blocking-bidirectional-conducting switches and it synthesizes a multilevel half-wave voltage waveform. The voltage stress on these switches is not distributed uniformly. The "polarity generation part" is a simple H-bridge connected at the output of the level generation part which generates negative and positive polarities for the output voltage. The switches in this part are unidirectional-blocking-bidirectional-conducting and have to with-stand the maximum voltage generated by the level generation part.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.6 Packed U-Cell Topology

these switches can be operated at line frequency. Thus these switches are high-voltage low-frequency switches.

A single-phase topology for a seven-level converter is shown in Fig. 3.7, where $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC}$. The operating states are listed in Table 3.7. It is evident that all possible combinations of the input voltage levels are not utilized. Thus, in this topology, equal load sharing among the input DC sources is not possible.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.7 Multilevel Module-Based MLI

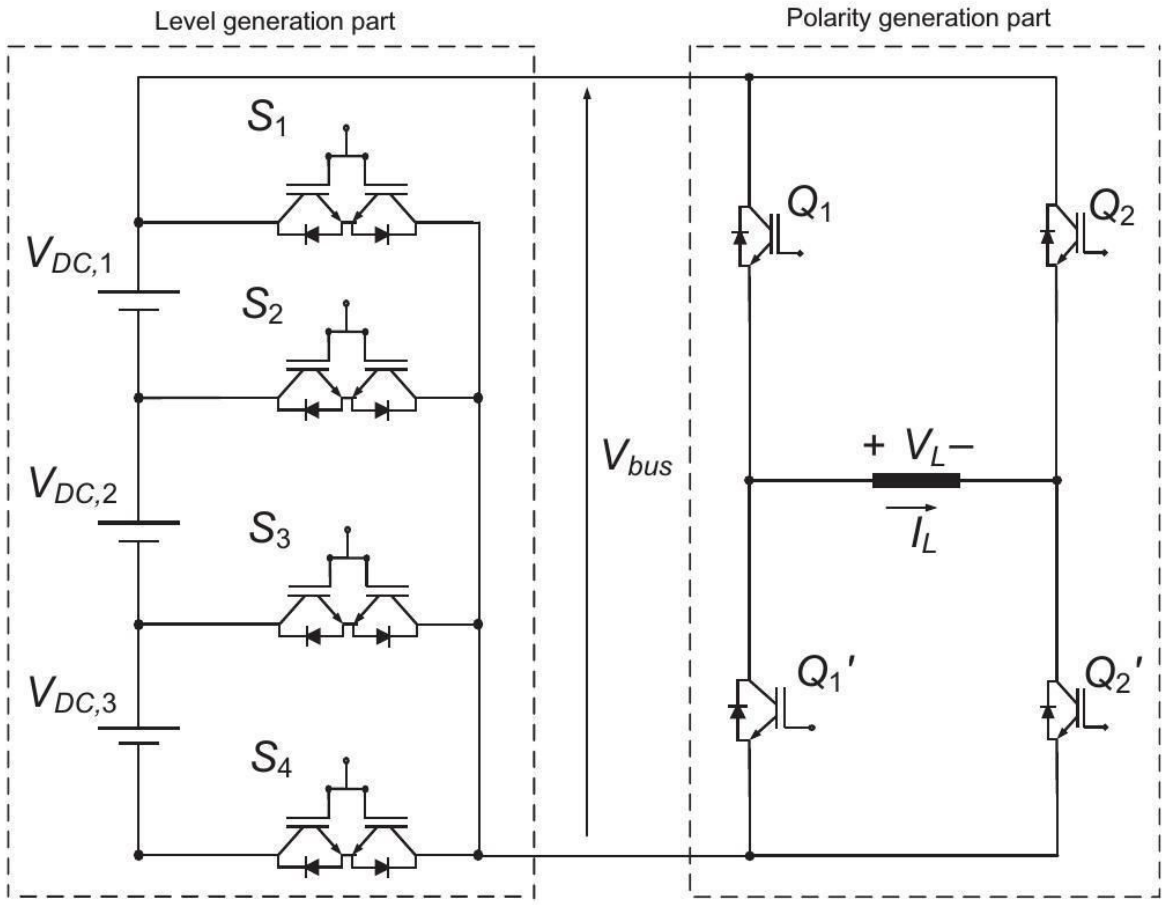


FIGURE 3.7 MLI topology as proposed in Reference [73].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.7 Multilevel Module-Based MLI

TABLE 3.7 Switching Combinations for the Topology Shown in Fig. 3.7

State	Output Voltage at Level Generation Part $V_{bus}(t)$	Switches in ON State (Other Switches Remain OFF)	Remarks
1	$V_{DC,1}$	S_2	
2	$V_{DC,2}$	S_1, S_2, S_3	Not possible as both $V_{DC,1}$ and $V_{DC,2}$ get short-circuited
3	$V_{DC,3}$	S_1, S_3, S_4	Not possible as $V_{DC,3}$ gets short-circuited
4	$V_{DC,1} + V_{DC,2}$	S_3	
5	$V_{DC,2} + V_{DC,3}$	S_1, S_2, S_4	Not possible as $V_{DC,1}$ gets short-circuited
6	$V_{DC,3} + V_{DC,1}$	S_2, S_3, S_4	Not possible as both $V_{DC,2}$ and $V_{DC,3}$ get short-circuited
7	$V_{DC,1} + V_{DC,2} + V_{DC,3}$	S_4	
8	0	S_1	

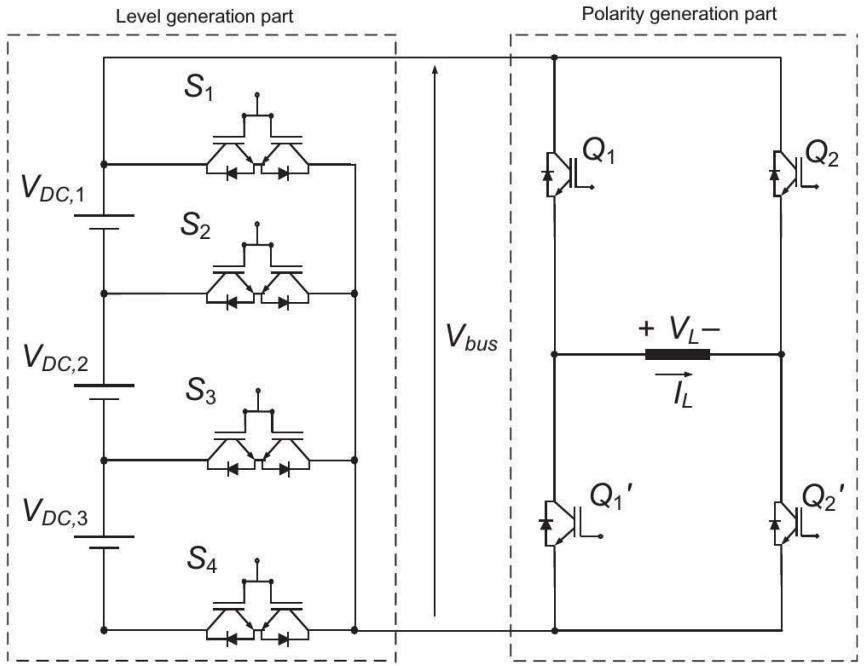


FIGURE 3.7 MLI topology as proposed in Reference [73].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.7 Multilevel Module-Based MLI

The switches in the H-bridge, Q_1, Q_2, Q_1', and Q_2', are each subjected to the voltage stress of $3V_{DC}$. Switches S_1 and S_4 need to have a minimum voltage-blocking capability of $3V_{DC}$, whereas switches S_2 and S_3 should be selected to bear the voltage stress of $2V_{DC}$. However, only one switch in the level generation part and two switches in the polarity generation part need to conduct simultaneously. The topology does not allow asymmetrical source configuration (binary or trinary), because it is not possible to synthesize all subtractive and additive combinations.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.8 Reversing Voltage Topology

3.3.8 Reversing Voltage Topology

The reversing voltage topology proposed in References [74,75] is illustrated in Fig. 3.8. It is a hybrid topology which separates the output voltage into two parts. One part synthesizes a multilevel stepped voltage half-wave. This part is named the "level generation part," comprising input DC sources $V_{DC,\ J}$ $\{j = 1-4\}$ and switches S_j $\{j = 1-8\}$. A full-bridge, comprising switches Q_j $\{j = 1-4\}$, is connected to the level generation part so as to obtain both positive and negative polarities for the output voltage. This part is named the "polarity generation part." In this way, the components are utilized effectively. The switches in the polarity generation part need to withstand the total additive voltage of the level generation part. This topology exhibits modularity for the level generation part.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.8 Reversing Voltage Topology

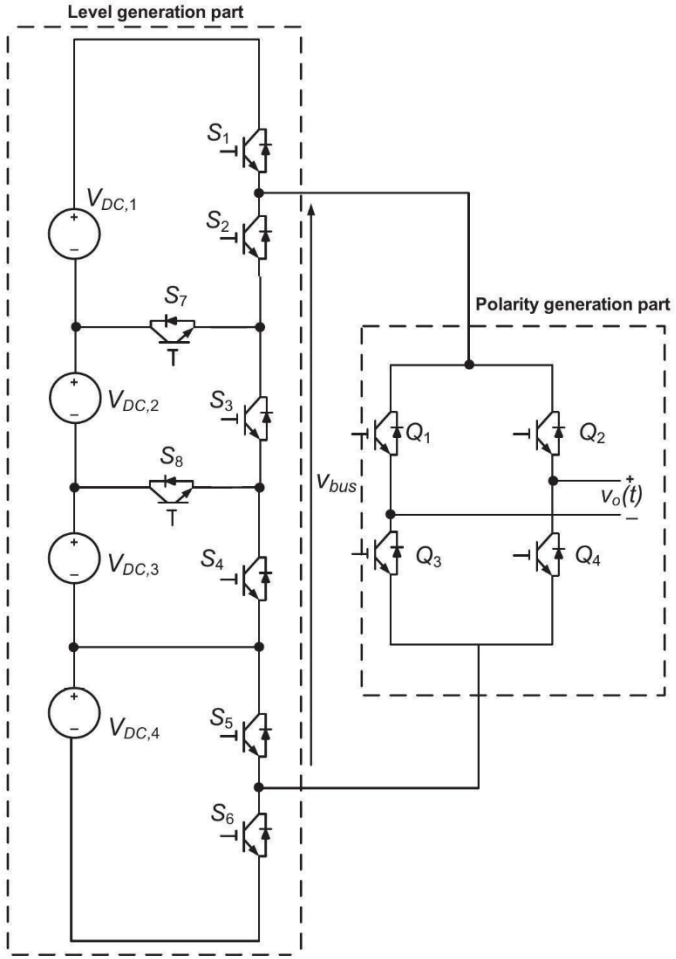


FIGURE 3.8 MLI topology as proposed in References [74,75].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.8 Reversing Voltage Topology

Various possible states to obtain different levels at the level generation part, $v_{bus}(t)$, are summarized in Table 3.8. It can be noted that the switches with high blocking voltages, Q_j $\{j = 1-4\}$, can be operated at fundamental switching frequency. If symmetric sources are used such that $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC}$, then all switches of the level generation part experience a voltage stress of V_{DC}, while the four switches of the polarity generation part are required to have a minimum voltage-blocking capability of $4V_{DC}$ each. It can also be inferred from Table 3.8 that for symmetric source configuration, equal load sharing amongst them is not possible.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.8 Reversing Voltage Topology

For a DC link created with connected capacitors, this limitation will affect voltage balancing in the capacitors. It can also be observed from Table 3.8 that the number of switches conducting simultaneously to synthesize a required voltage level is not the same, and thus conduction losses and switching losses for the switches may not be the same. Moreover, since the topology does not facilitate the synthesis of all additive and subtractive combinations of input voltage sources, trinary source combinations cannot be used.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.8 Reversing Voltage Topology

Employing other asymmetric combinations to maximize the number of output levels is seriously hampered by the absence of some states with a single voltage source (e.g., as seen from Table 3.8, using State 2 for engaging the source $V_{DC,2}$ would lead to short-circuiting of source $V_{DC,3}$ and hence this state cannot be used). However, one important advantage that the topology offers is that it uses a single DC link for three-phase implementation.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.8 Reversing Voltage Topology

TABLE 3.8 Possible Switching Combinations for the Topology Shown in Fig. 3.8

State	Output Voltage at Level Generation Part $v_{bus}(t)$	Switches in ON State (Other Switches Remain OFF)	Remarks
1	$V_{DC,1}$	S_1, S_3, S_4, S_5, S_7	–
2	$V_{DC,2}$	S_2, S_4, S_5, S_7, S_8	Not possible as $V_{DC,3}$ gets short-circuited
3	$V_{DC,3}$	S_2, S_3, S_5, S_8	–
4	$V_{DC,4}$	S_2, S_3, S_4, S_6	–
5	$V_{DC,1} + V_{DC,2}$	S_1, S_4, S_5, S_8	–
6	$V_{DC,2} + V_{DC,3}$	S_2, S_5, S_7	–
7	$V_{DC,3} + V_{DC,4}$	S_2, S_3, S_6, S_8	–
8	$V_{DC,1} + V_{DC,4}$	S_1, S_3, S_4, S_6, S_7	–
9	$V_{DC,2} + V_{DC,4}$	S_2, S_4, S_6, S_7, S_8	Not possible as $V_{DC,3}$ gets short-circuited

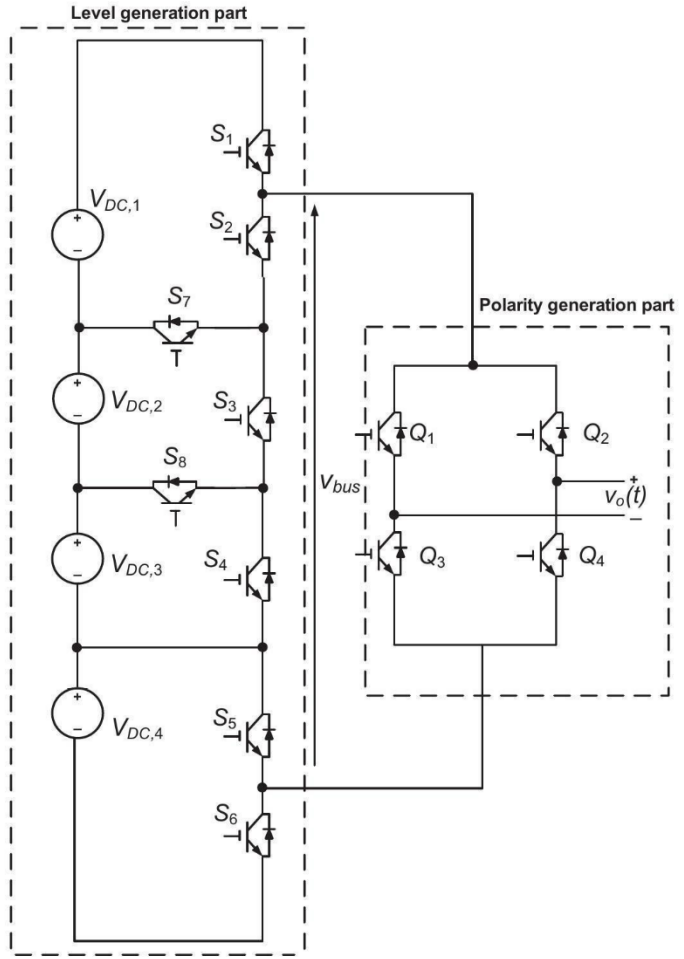


FIGURE 3.8 MLI topology as proposed in References [74,75].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

TABLE 3.8 Possible Switching Combinations for the Topology Shown in Fig. 3.8

State	Output Voltage at Level Generation Part $v_{bus}(t)$	Switches in ON State (Other Switches Remain OFF)	Remarks
10	$V_{DC,1} + V_{DC,3}$	S_1, S_3, S_5, S_7, S_8	Not possible as $V_{DC,2}$ gets short-circuited
11	$V_{DC,1} + V_{DC,2} + V_{DC,3}$	S_1, S_5	–
12	$V_{DC,2} + V_{DC,3} + V_{DC,4}$	S_2, S_6, S_7	–
13	$V_{DC,1} + V_{DC,3} + V_{DC,4}$	S_1, S_3, S_6, S_7, S_8	Not possible as $V_{DC,2}$ gets short-circuited
14	$V_{DC,1} + V_{DC,2} + V_{DC,4}$	S_1, S_4, S_6, S_8	Not possible as $V_{DC,3}$ gets short-circuited
15	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4}$	S_1, S_6	–
16	0	S_2, S_3, S_4, S_5	–

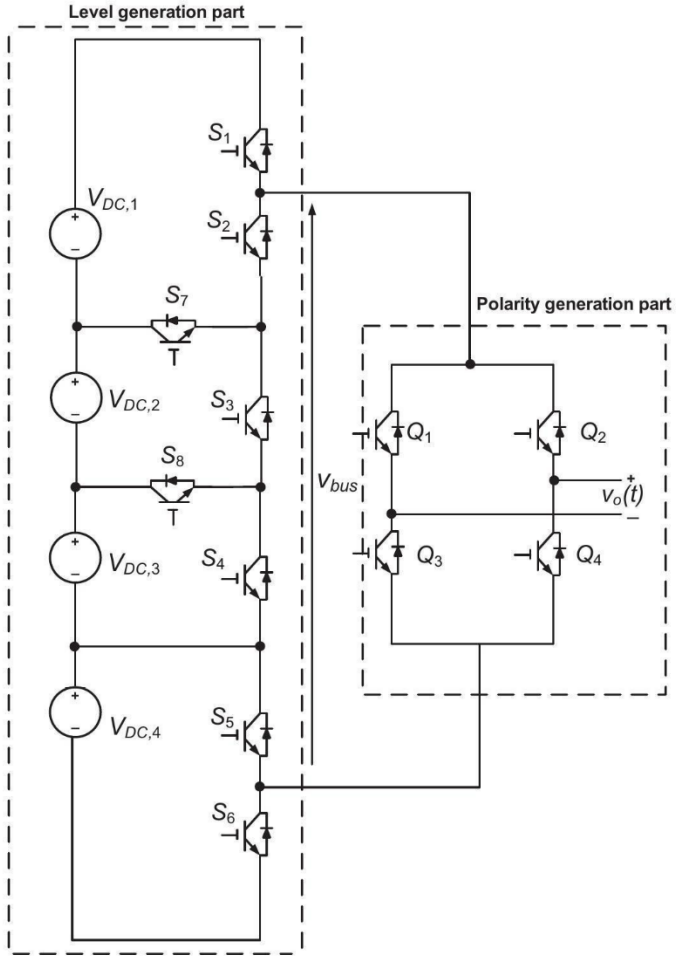


FIGURE 3.8 MLI topology as proposed in References [74,75].

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.9 Two-Switch Enabled Level Generation-Based MLI

3.3.9 Two-Switch Enabled Level Generation–Based MLI

The topology presented by Babaei [76] requires a mix of unidirectional and bidirectional switches, as shown in Fig. 3.9. It also consists of two parts, wherein one part helps in the generation of voltage levels and the other takes part in the generation of polarities. The level generation part requires both unidirectional and bidirectional switches. However, this part is unable to synthesize the zero level. The polarity generation part is an H-bridge with unidirectional switches. These switches operate under the voltage stress equal to the maximum voltage generated at $V_{bus}(t)$. Since the level generation part is not able to synthesize the zero level, the switches in the H-bridge cannot be operated at line frequency.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

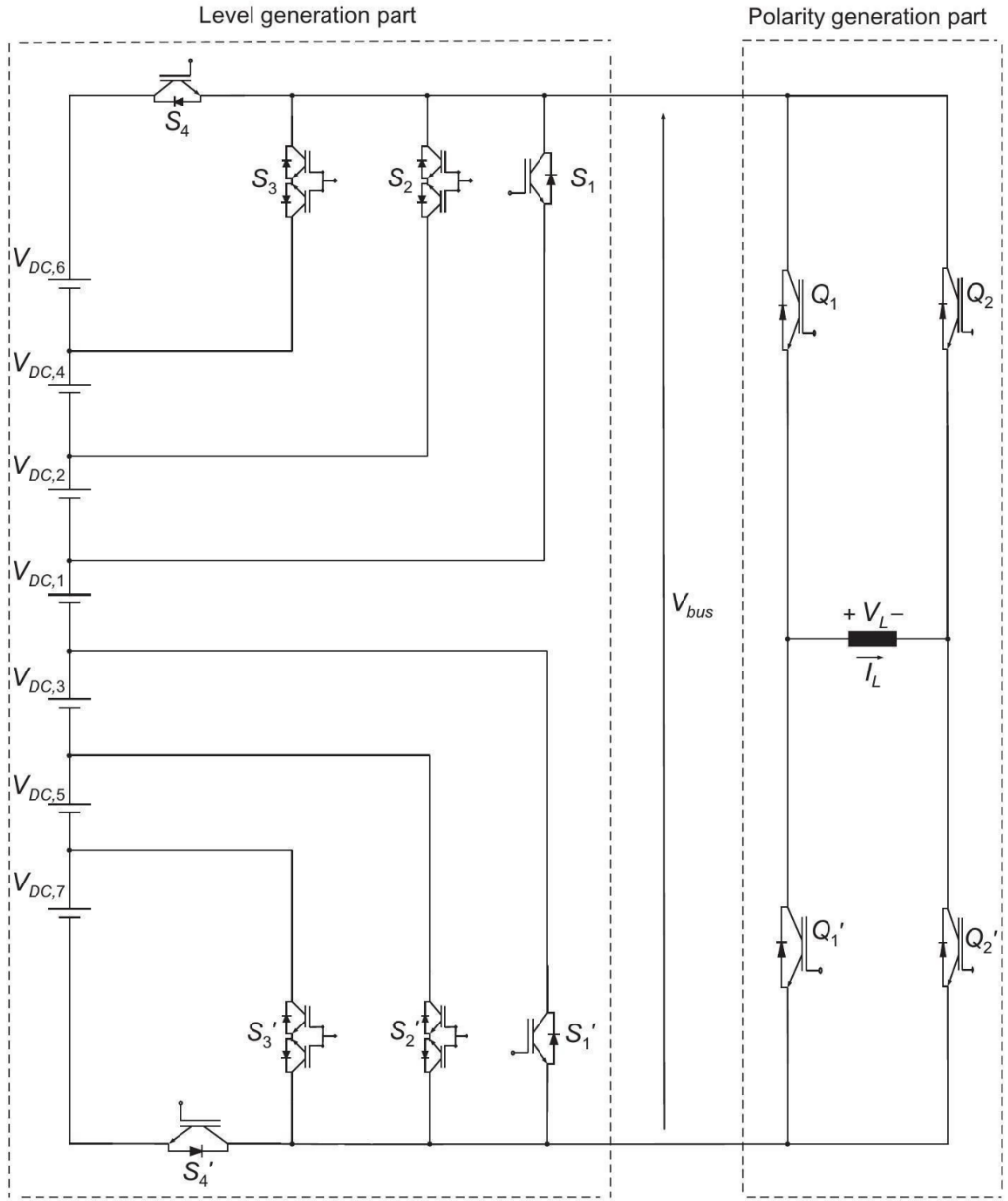


FIGURE 3.9 MLI topology as proposed in Reference [76].

TABLE 3.9 Switching States for Topology Shown in Fig. 3.9

State	Output Voltage at Level Generation Part $V_{bus}(t)$	Switches in ON State (Other Switches Remain OFF)
1	$V_{DC,1}$	S_1, S_1'
2	$V_{DC,1} + V_{DC,2}$	S_2, S_1'
3	$V_{DC,1} + V_{DC,2} + V_{DC,3}$	S_2, S_2'
4	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4}$	S_3, S_2'
5	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4} + V_{DC,5}$	S_3, S_3'
6	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4} + V_{DC,5} + V_{DC,6}$	S_4, S_3'
7	$V_{DC,1} + V_{DC,2} + V_{DC,3} + V_{DC,4} + V_{DC,5} + V_{DC,6} + V_{DC,7}$	S_4, S_4'

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.9 Two-Switch Enabled Level Generation-Based MLI

A single-phase structure with seven input DC voltage sources is shown in Fig. 3.9. For a symmetrical source configuration, $V_{DC,1} = V_{DC,2} = V_{DC,3} = V_{DC,4} = V_{DC,5} = V_{DC,6} = V_{DC,7} = V_{DC}$. Table 3.9 lists the various operating states for the given structure. It can be observed that only two switches are conducting per state in the level generation part, and hence it is called "two-switch enabled level generation-based MLI." The zero level is synthesized using the H-bridge. It is not possible to apply the concept of charge balancing in this topology as all the sources do not contribute equally for each level in the $V_{bus}(t)$.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.3.9 Two-Switch Enabled Level Generation-Based MLI

The switches in the H-bridge, Q_1, Q_2', Q_1', and Q_2, need to have a minimum voltage-blocking capability of $7V_{DC}$. Switches S_1, S_4, S_1', and S_4', of the level generation part need to have a minimum voltage-blocking capability of $3V_{DC}$. The remainder of the switches need to have a minimum voltage-blocking capability of $2V_{DC}$ .It is also observed that this topology does not support asymmetrical source configuration (binary or trinary) as it is not possible to synthesize all subtractive and additive combinations of the input voltage levels. However, one advantage that this topology offers is that a total of four power electronic switches need to be conducting in any state, resulting in lower conduction losses.

Thus, the description of topologies proposed for reducing the component count indicates that a given structure has its pros and cons.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.4 Summary

3.4 SUMMARY

As MLIs continue to gain increasing importance for both high-power and low-power applications, many researchers have proposed specific topological solutions for intended applications. Also, new multilevel topologies have been proposed offering high output resolution with a reduced number of devices. Based on the discussion on new topologies, it can be concluded that in the process of reducing the device count, various compromises are involved which affect the topology characteristics, such as:

1. the possibility of charge balance control (equal load sharing amongst the input sources);
2. optimal switching of the differently rated power switches; and
3. the possibility of asymmetric source configuration.

روش‌های نوین کنترل مبدل‌های الکترونیک قدرت

✓ فصل ۳ [۱]: ظهور ساختارهای جدید

❖ 3.4 Summary

In this book, topological solutions will be further explored which can preserve the desired characteristics, while reducing the device count for voltage output with a large number of levels. In addition, a comparison of these topologies will be carried out with the classical topologies in terms of the number of power switches, isolated sources/capacitors, clamping components, voltage stresses, etc.